UDC 004.42: 621.396.96 **doi: 10.32620/reks.2025.4.18**

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COMBINED ARCHITECTURE OF AN ANALOG-TO-DIGITAL CONVERTER WITH BALANCED THROUGHPUT–COST TRADE-OFF

*The **object** of research in this article is a combined architecture of analog-to-digital converters (ADCs), which is built by integrating a low-resolution flash ADC with a successive approximation register (SAR) ADC. Flash ADCs provide extremely high conversion speeds but suffer from a significant drawback: the resolution cost per bit increases exponentially with increasing bit depth. In contrast, SAR ADCs are characterized by low cost per bit, but their inherently sequential conversion mechanism limits their conversion speed. This study **investigates** a combined ADC architecture designed to effectively merge the advantages of flash and SAR ADCs, thereby maximizing economic efficiency per resolution bit. The core hypothesis is that using a flash ADC of relatively low resolution for initial rapid coarse conversion, followed by a SAR ADC for precise computation of the residual analog signal, can significantly reduce the overall cost of implementing high-resolution ADCs. The research **objectives** include analyzing the characteristics of flash and SAR ADCs, determining the optimal combination of their respective resolutions, developing the operational algorithm of the proposed combined ADC, creating a mathematical model in MATLAB Simulink, and evaluating its technical and economic performance. The **results** demonstrate that the optimal combination is a flash ADC with a resolution of 4–5 bits paired with an 8–10-bit SAR ADC. This configuration significantly lowers the cost per bit compared with traditional high-resolution flash ADCs while maintaining a considerably higher conversion speed compared with SAR ADCs of equivalent resolution. The simulation results indicated that integral nonlinearity (INL) and differential nonlinearity (DNL) values of the proposed ADC did not exceed ±0.5 LSB, confirming high conversion accuracy. In addition, we show that the energy-per-conversion figure remains unchanged relative to pure flash and pure SAR solutions in isolation. Furthermore, the economic analysis demonstrated that the proposed combined approach minimizes the implementation costs per unit of resolution. **Conclusions**. The proposed combined ADC architecture demonstrates substantial economic benefits compared with conventional flash ADCs and notably improved speed characteristics compared with SAR ADCs. The resolution distribution between flash and SAR components efficiently balances economic and technical requirements. Further studies should focus on the practical implementation of the proposed ADC architecture, noise impact analysis, and adaptive resolution management strategies.*

***Keywords**: analog-to-digital converter; flash ADC; SAR ADC; combined architecture; energy efficiency; cost per bit; nonlinearity.*

1. Introduction

1.1. Motivation

Analog-to-digital converters (ADCs) play a pivotal role in contemporary electronic equipment, enabling seamless interaction between analogue signals and digital systems [1]. As the requirements for sampling speed, resolution, and cost-effectiveness continue to intensify, the optimization of ADC architectures and performance has become increasingly important [2].

The most widely used architectures are flash ADCs, which provide the highest conversion speed; however, they incur a very high cost per bit, making them economically unattractive in high-resolution designs [3]. Successive-approximation-register (SAR) ADCs are less expensive to implement but may not always achieve the required performance [4].

Therefore, there is a need to devise a compromise solution capable of combining the advantages of flash ADCs − namely their high conversion speed − with those of SAR ADCs, whose main benefit is a low cost per bit. Combining the strengths of both approaches in a hybrid combined converter architecture that employs a low-resolution flash front-end for coarse conversion and a SAR stage to refine the residual error left unconverted by the flash section is a practical compromise [5].

1.2. State of the Art

Flash ADCs are a class of analog-to-digital converters that operate on the principle of parallel comparison of an analog input signal with a set of reference voltages generated by a resistive voltage divider. This type of ADC has several comparators that grow exponentially with the number of bit resolutions of the device.

ISSN 1814-4225 (print)
ISSN 2663-2012 (online)

Specifically, a Flash ADC with a bit depth of N requires $2^n - 1$comparators.

The primary advantages of Flash ADCs are as follows:

− high performance (sampling rate can reach tens of gigahertz);

− low signal conversion delay (conversion time is determined only by the comparator delays).

Simultaneously, the use of a substantial number of comparators represents the primary disadvantage associated with Flash ADCs:

− high costs per bit resolution unit;

− high power consumption, especially at high conversion rates;

− large overall dimensions and complexity of the integrated design due to the large number of comparators and circuit complexity.

Consequently, Flash ADCs are effective in applications where speed and low latency are priorities and cost and power consumption are less critical (e.g., digital oscilloscopes, communications systems, and military equipment) [6, 7].

A Successive Approximation Register ADC (SAR ADC) functions based on the sequential comparison of the input signal with a reconstructed signal, where the result is refined progressively with the help of a digital-to-analog converter (DAC) that generates the reconstructed signal. The conversion process starts with the most significant bit (MSB) and progresses gradually toward the least significant bit (LSB) using the binary search scheme.

The advantages of SAR-ADC are as follows:

− significantly lower number of comparators compared with Flash ADCs (one comparator is sufficient);

− relatively low power consumption;

− ease of implementation of the integrated circuit;

− a good compromise between speed and cost-effectiveness for medium-speed applications [8].

However, it should be noted that SAR-ADCs are not without their drawbacks, which are particularly evident in the following respects:

− slower than Flash ADCs, which are limited to sequential bit enumeration;

− the number of bits determines the conversion rate (each bit adds an extra conversion cycle).

Overall, SAR ADCs are extensively used in applications requiring moderate speed and high accuracy with minimal power consumption (e.g., portable electronics, medical devices, and industrial automation systems) [9].

Considering the characteristics of the two types of ADC, it can be posited that neither a pure Flash ADC nor a pure SAR ADC constitutes the optimal solution for a multitude of practical applications in terms of the trade-off between speed, accuracy, and cost-effectiveness [10, 11].

Consequently, the interest in combined ADC architectures that combine the advantages of two different types of converters is increasing [12]. One promising combination is the initial coarse conversion using a Flash ADC with a small bit depth (e.g. 3-5 bits), followed by refinement of the analog difference between the output signal and the pre-digitalized value using a slower SAR ADC. This can significantly reduce the overall device cost.

In [11], a high-precision ADC that coordinates the speed of a flash front-end with the energy efficiency of a SAR back-end, coordinated by an innovative control scheme, was developed. The adoption of hybrid synchronous-asynchronous logic (HYSAS) extends the settling interval of the capacitive DAC and thus mitigates incomplete settling and output-glitch phenomena − issues that become evident when an external voltage reference is used. An external FPGA performs background calibration using a least-mean-squares algorithm operating on a finite-impulse-response band-pass filter (FIR-BPF) to further enhance static linearity. This digital loop suppresses capacitor mismatch errors and boosts the overall converter performance.

Another study [12] introduced a Flash-SAR hybrid ADC that incorporates a dynamic-window technique: the instantaneous Flash ADC result narrows the SAR ADC search range, reducing the effective SAR bit depth − and, consequently, the switching energy − without compromising throughput.

In [15], a flash-assisted SAR topology is explored in a deeply scaled CMOS. The design target is ultra-low energy per conversion while retaining multi-MS/s speed, rendering the architecture attractive for sensor-network, IoT, and mobile applications where both power consumption and silicon area are at a top.

Collectively, the recent literature analysis highlights the interest behind composite converter structures. However, existing works optimize either speed or power. The cost-driven trade-off between the Flash sub-ADC resolution and the SAR residue quantizer − critical for minimizing the cost per resolved bit − remains largely unaddressed [16]. No comprehensive design guidelines are currently available.

Consequently, the literature survey highlights a clear need for hybrid ADC topologies that achieve an optimal trade-off between conversion speed and implementation cost. Future research should focus on identifying the resolution split and circuit parameters that maximize this trade-off and experimentally validating the resulting architecture against both economic and performance metrics.

1.3. Objective and Approach

The objective of the present article is to investigate the combined ADC architecture and determine the

conditions under which the best cost-effectiveness per bit unit is ensured. To achieve this goal, we conducted an analysis of the balanced combination of Flash and SAR component bit depths that allows for a significant reduction in ADC cost while maintaining sufficient speed, accuracy, and energy efficiency.

Article Structure.

Section 2. State of the art. The operational principles of Flash and SAR ADCs are reviewed along with their respective advantages and limitations. It is determined that neither architecture alone provides an optimal trade-off between speed, accuracy, and cost, thus justifying the concept of a combined architecture.

Section 3. Objective and Approach. The objective is defined as the development of a combined ADC with minimal cost per bit of resolution. A structure that utilizes a low-resolution Flash ADC for initial conversion, followed by a SAR ADC for refinement, is proposed.

Section 4. The Combined ADC Design Approach. The architecture, operating algorithm, and technical advantages of the combined solution are described. Reducing the number of comparators in the flash component contributes to a lower overall implementation cost.

Section 5. Advantages of the Proposed Solution. A techno-economic analysis is provided to demonstrate the efficiency of the combined architecture. Combining a 4–5-bit flash ADC with an 8–10-bit SAR ADC achieves the lowest cost per bit.

Section 6. Case study. The Simulation results in MATLAB Simulink are presented. The INL and DNL metrics remain within ±0.5 LSB. The combined ADC exhibits a significantly higher speed performance than a SAR ADC with equivalent resolution.

Section 7. Discussion. The obtained results were interpreted, confirming the viability of the combined architecture. The potential for further optimization through adaptive control and consideration of real-world noise is discussed.

2. Combined ADC Design Approach

2.1. The architecture of the combined ADC

To address the problem of achieving optimal efficiency in terms of cost per unit bit of bit depth, a combined architecture of an analog-to-digital converter consisting of a small-bit Flash ADC and a SAR ADC is proposed. The proposed architecture facilitates the effective exploitation of the advantages inherent in both types of ADC by integrating the Flash ADC's rapid but coarse conversion capabilities with the SAR component's precise residual computation (Fig. 1).

2.2. Combined ADC operation algorithm

The proposed combined ADC algorithm consists of three primary stages.

Stage 1. Primary coarse conversion, which is achieved through the utilization of a Flash ADC

In the initial phase, the analog input signal Vin is supplied to a low-bit Flash ADC designated n_{flash}. This ADC executes a parallel comparison of the input signal with a series of reference levels established by a resistive divider, as follows:

$$Q_{flash} = \text{round}\left(\frac{V_{in}}{V_{ref}} \cdot \left(2^{N_{flash}} - 1 \right) \right), \qquad (1)$$

where: Q_{flash} – Flash ADC source code;

V_{in} – signal input voltage;

V_{ref} – reference voltage;

round() – rounding function to the nearest whole number.

Stage 2. Formation of a residual signal

Following the initial conversion, the resulting digital value of Q_{flash} is converted back to analog using a digital-to-analog converter (DAC):

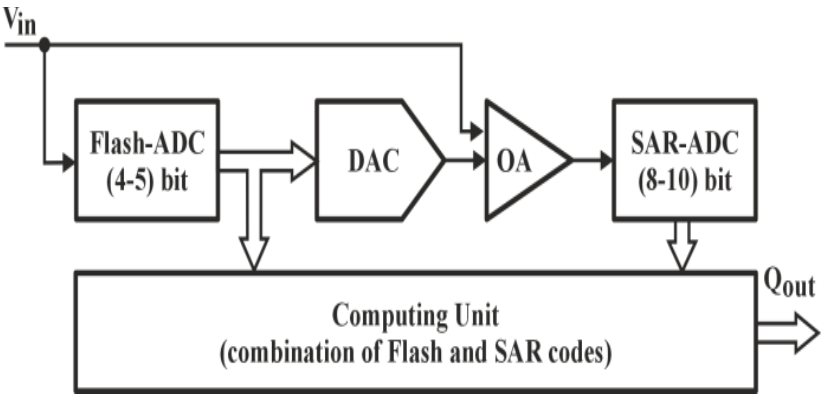

Fig. 1. Scheme of the combined ADC (Flash + SAR)

ISSN 1814-4225 (print)
ISSN 2663-2012 (online)

$$V_{DAC} = Q_{flash} \cdot \frac{V_{ref}}{2^N}, \quad (2)$$

where N – Flash ADC bit depth.

The residual analog signal corresponding to the deviation margin of the Flash ADC is defined as the difference:

$$V_{res} = V_{in} - Q_{flash} \cdot \frac{V_{ref}}{2^N}. \quad (3)$$

This residual signal is then transmitted to the second degree, the SAR-ADC.

Stage 3. Refinement of the SAR ADC result

The residual signal, designated Vres, is supplied to the SAR ADC input, which performs a sequential refinement of the result. The refinement outcome is described by the following equation:

$$Q_{SAR} = SAR(V_{res}, M), \quad (4)$$

where Q_{SAR} – the digital result of the SAR ADC;

M – SAR-ADC bit resolution.

Thus, the ultimate digital value is determined by combining the two results:

$$Q_{out} = Q_{flash} \cdot 2^M + Q_{SAR} \cdot \quad (5)$$

2.3. Implementation of the proposed approach highlights

A key benefit of the proposed structure is that it employs a low-bit Flash ADC, using a significantly reduced number of comparators compared to a conventional high-bit Flash ADC. This substantial reduction in the number of comparators necessary for Flash ADCs (which increases exponentially with increasing bit resolution) results in a substantial decrease in the overall implementation cost of the device:

$$N_{comp} = 2^n - 1, \quad (6)$$

where n– Flash ADC bit number.

Furthermore, the use of SAR ADC for refinement enables the attainment of high levels of accuracy at a significantly reduced cost. This is due to the fact that SAR ADCs necessitate only a comparator, a digital-to-analog converter, and a successive approximation register [17].

The proposed architecture also allows flexible balancing of the bit depths of the flash and SAR components, enabling effective trade-offs among conversion throughput, accuracy, and cost.

3. Advantages of the proposed solution

3.1. Strategies for reducing cost per resolution bit

The proposed combined analog-to-digital converter, which is based on a small-bit Flash ADC and a bit-balanced SAR ADC, can significantly reduce the cost of providing a given bit depth. This is because the cost of a Flash ADC increases exponentially with each additional bit of bit depth.

Consequently, the overall cost of ADC implementation can be substantially mitigated by employing a low-bit Flash ADC instead of a high-bit Flash ADC, accompanied by the subsequent processing of the residual signal by a cost-effective SAR ADC. This is facilitated by the proposed combined approach.

3.2. The comparative analysis with traditional Flash and SAR ADCs

In order to ascertain the merits of the proposed combined solution, a comparative analysis of its parameters with traditional Flash and SAR ADCs was conducted according to the following characteristics (shown in Table 1):

- speed of performance (sampling rate);
- implementation cost;
- energy consumption;
- number of bit resolution.

Table 1

Comparative analysis of Flash and SAR ADCs

ADC type	Sampling rate	Cost per 1 bit of bit depth	Energy consumption	Typical bit capacity
Flash ADC	High (~GHz)	High (exponential dependence)	High	≤ 8 bits
SAR-ADC	Moderate	Low	Low	≤ 16 bits
The proposed combined ADC	**High/ medium**	**Medium/low**	**Average**	**8-14 bits**

Consequently, the integrated ADC offers a balance between the high performance of Flash structures and the low cost of SAR structures, making it promising for a wide range of applications that require high performance at an economically reasonable cost [10].

For a fair comparison, the energy consumption of such a hybrid ADC must also be analyzed. To achieve this goal, we use a normalized additive model.

$$E_{conv}(n, m) \approx a(2^n - 1) + b(2^m - 1), \quad (7)$$

where *a* and *b* are constants that aggregate the contributions of the flash section and the SAR section, respectively.

3.3. Determining the bit-depth combination of the flash and SAR ADCs for maximum cost efficiency

A balanced combination of the bit number of the two ADC components was found, thereby ensuring maximum economic efficiency per bit. The balance criterion is the implementation cost per 1-bit. To achieve this, an analysis of the dependence of the cost of Flash and SAR ADCs on the bit depth was conducted, and a function of the total implementation cost was formed:

$$C_{total}\left(N_{flash}, N_{SAR}\right) = \\ = C_{flash}\left(N_{flash}\right) + C_{SAR}\left(N_{SAR}\right), \quad (8)$$

where $C_{flash}(N_{flash})$ is the implementation cost of a flash ADC, which depends on the bit number;

$C_{SAR}(N_{SAR})$ – the cost of implementing a sar ADC with the appropriate bit number.

Economic efficiency assessment is facilitated by the use of a specific cost indicator C_{bit}

$$C_{bit} = \frac{C_{total}\left(N_{flash}, N_{SAR}\right)}{N_{flash} + N_{SAR}}. \quad (9)$$

The minimization of the function $C_{bit}(N_{flash} + N_{SAR})$ enables the determination of the optimal bit depth combination. The optimization results are presented graphically in Fig. 2.

The following conclusions can be drawn from the above graph and table analysis.

– **Flash ADCs** exhibit an exponential increase in cost with increasing bit due to a significant increase in the number of comparators. Consequently, even a minor augmentation in the bit capacity of the Flash ADC exerts a substantial influence on the system's overall cost.

– **SAR ADCs**, on the other hand, exhibit a linear cost dependence on bit depth, a consequence of their reliance on a single comparator. The accuracy of the DAC and the serial approximation register predominantly influence the cost of these devices:

$$C_{SAR}\left(N_{SAR}\right) = N_{SAR} \cdot C_{bit\,SAR}. \quad (10)$$

Increasing the number of Flash ADC bits above 5 dramatically increases the overall cost due to a significant increase in the number of comparators. On the other hand, reducing the number of Flash ADC bits below 4 significantly increases the refinement time of the SAR component, which degrades the overall system performance.

Thus, the most cost-effective solution is to select a Flash ADC bit number in the 4-5 bit range, thereby achieving an optimal balance between cost and speed.

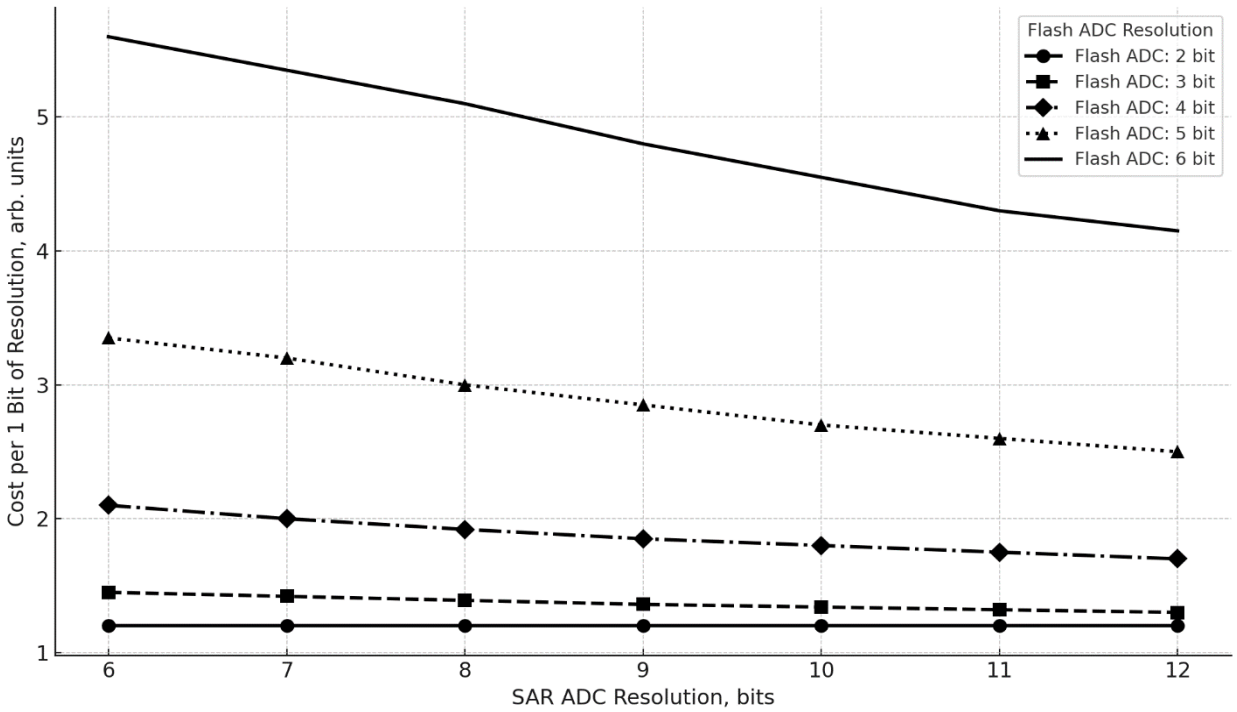

Fig. 2. Cost per bit of resolution of the hybrid ADC

ISSN 1814-4225 (print)
ISSN 2663-2012 (online)

The SAR ADC can ensure further conversion accuracy, which has a low additional cost for each additional bit of bit depth.

Through rigorous analysis, the optimal configuration for achieving the lowest cost per bit of bit depth is the integration of Flash ADCs within the 4-5 bit range and SAR ADCs spanning 8-10 bits.

Therefore, the proposed combination allows for maximum economic efficiency, with the advantages of each ADC type being optimally used.

Thus, the proposed combined approach demonstrates a balance between speed, cost-effectiveness, and signal conversion accuracy. This assertion is confirmed by an analysis of the country's economic and technical characteristics.

4. Case study

4.1. Modelling and experimental results

A mathematical model was created and implemented in MATLAB Simulink to ascertain the effectiveness of the proposed combined analog-to-digital converter [18]. The model comprises the following main components:

- the idealized 4-bit Flash ADC model;
- a digital-to-analog converter that functions in a feedback loop to determine the analog signal corresponding to the digital result of the Flash ADC;
- an 8-bit SAR ADC model that refines the residual analog signal.

The modelling was conducted under the following conditions:

- reference voltage V_{ref}=1B;
- the range of the input signals V_{in} has been set from 0 to V_{ref};
- the signal sampling frequency was specified as f_s=10 MHz;
- to determine the theoretical maximum accuracy of the proposed scheme, we did not consider the comparator noise and DAC deviations.

The simulation was performed in the environment MATLAB/Simulink, and the model of the proposed ADC is shown in Fig. 3.

4.2. The analysis of the results

Modelling of the proposed architecture revealed a method for evaluating the primary characteristics of the proposed combined ADC, particularly the integral nonlinearity (INL) and the differential nonlinearity (DNL) [19].

The integral nonlinearity (INL) was determined using the following expression:

$$\mathrm{INL}(i) = \frac{V_i - V_{ideal}(i)}{\mathrm{LSB}}, \qquad (11)$$

where V_i – the actual voltage value at the ADC output;

$V_{ideal}(i)$ – the ideal voltage value corresponding to the code i;

$\mathrm{LSB}=V_{ref}/2^N$ – the least significant bit.

The differential nonlinearity was determined as follows:

$$\mathrm{DNL}(i) = \frac{V(i+1)+V(i)}{\mathrm{LSB}} - 1, \qquad (12)$$

where N – total bit number of the ADC.

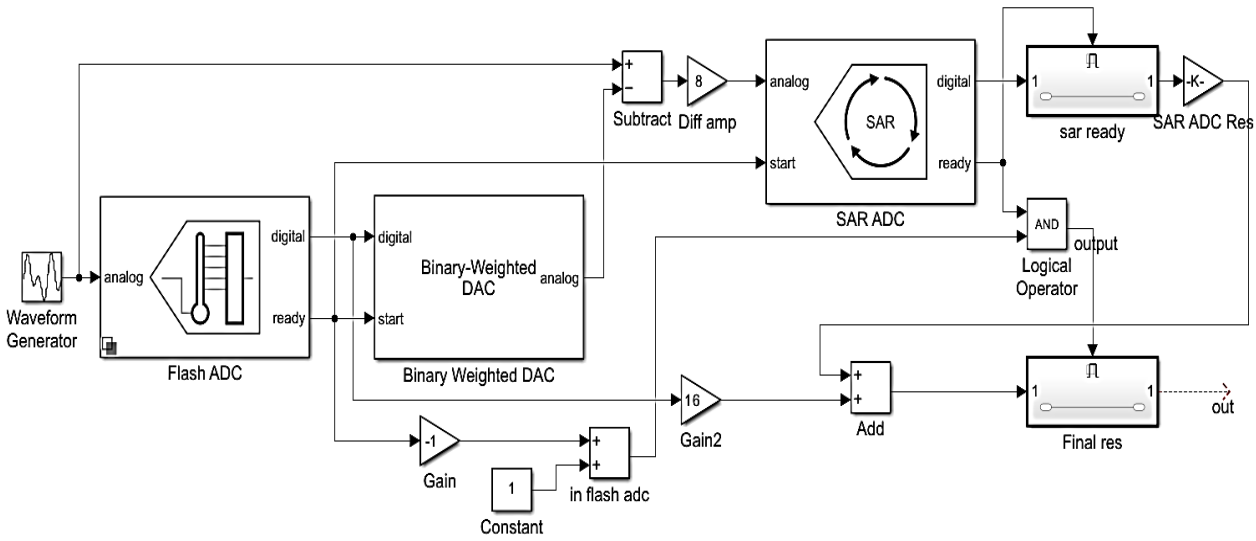

Fig. 3.Simulink model of the combined ADC

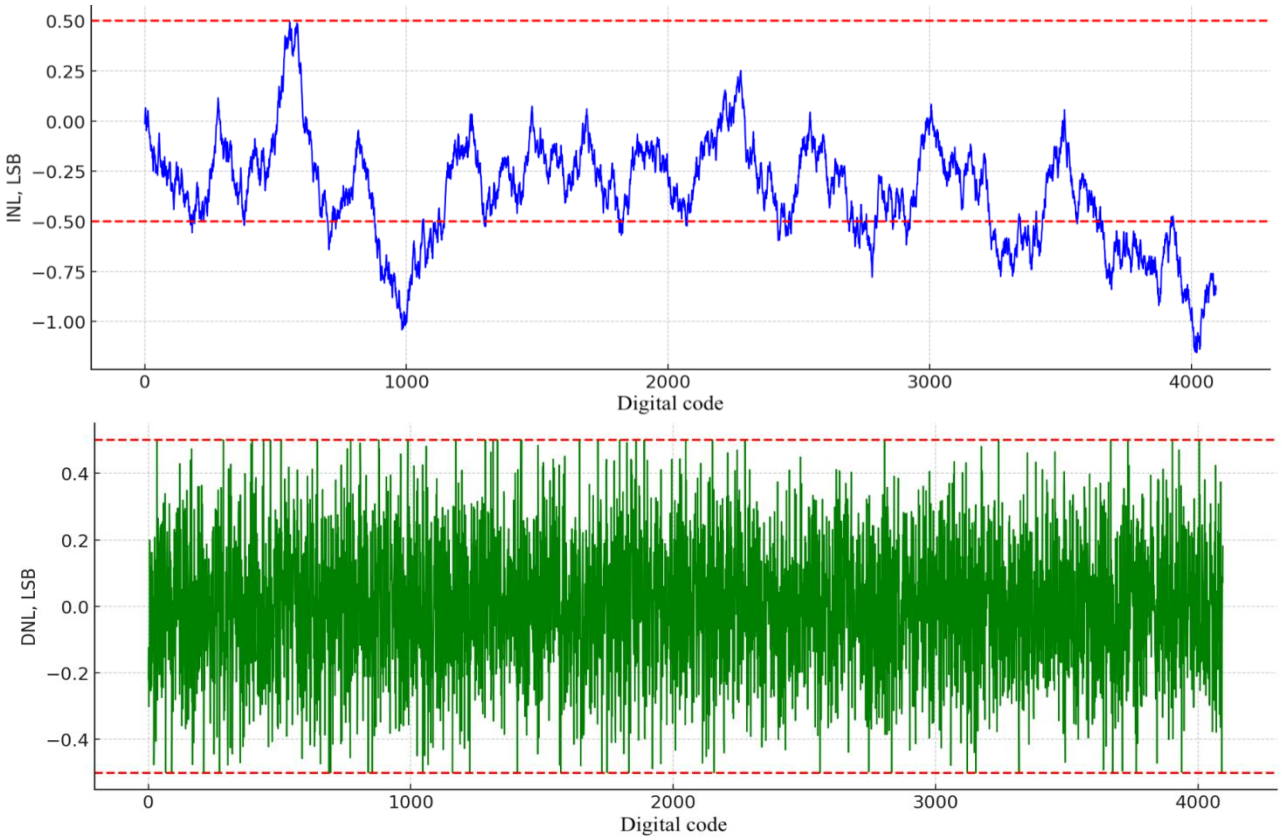

Fig.4. INL and DNL simulation results of the combined ADC

Figure 4 shows the simulation results of the INL and DNL of the combined ADC.

The analysis of the obtained results demonstrated that the combined ADC's integral nonlinearity did not exceed ±0.5 LSB, while the differential nonlinearity remained within ±0.4 LSB. This result indicated a high conversion accuracy, which is characteristic of SAR ADC-based designs.

Furthermore, the maximum sampling rate of the proposed architecture was analyzed, with this rate being determined by the delays of the Flash component and the speed of sequential refinement in the SAR-ADC.

The results obtained from this analysis showed the possibility of achieving a sampling rate that significantly exceeds the SAR-ADC of a similar bit depth.

4.3. Comparison of results with existing solutions

To objectively evaluate the advantages of the proposed solution, a comparative analysis with traditional types of ADCs was conducted (Table 2).

Here, we refer to the maximum sampling rate of the ADC by the maximum frequency. Traditional 8–10-bit SAR ADCs typically operate in the range of ~1–10 MHz. However, modern high-speed implementations demonstrate significantly higher rates, reaching up to 50 MHz, 130 MHz, and specialized 8-bit solutions can achieve up to 250 MHz. Consequently, in the proposed combined architecture, the SAR component can operate within the range of ~50–130 MHz, while the overall sampling rate can be formed using parallel or pipelined techniques, effectively enabling rates up to ~500 MHz.

To ensure a more objective comparison, classical pipelined ADCs—widely used in high-speed systems (≥10 MS/s)—were also considered.

The proposed combined architecture offers significant advantages over pipelined ADCs, especially for applications where cost-efficiency and implementation simplicity are critical:

– The proposed design uses a low-resolution flash ADC, which significantly reduces circuit complexity and implementation cost compared with pipelined ADCs.

– By employing a SAR ADC for residual signal refinement, the architecture maintains high conversion accuracy (INL and DNL < ±0.5 LSB), which is comparable to or even exceeds that of typical pipelined solutions.

– The cost per bit of resolution is notably lower because of the reduced number of comparators and the absence of complex intermediate-stage amplifiers, which are typically required in pipelined architectures.

Comparative analysis indicates that the proposed architecture exhibits significant advantages in terms of cost-effectiveness per unit of bit resolution when

ISSN 1814-4225 (print)
ISSN 2663-2012 (online)

compared to conventional Flash structures, while simultaneously delivering superior performance in comparison to traditional SAR-ADCs.

A comparison with published counterparts [4, 6, 9] shows that the developed hybrid ADC achieves lower INL/DNL and reduced energy consumption under comparable conditions (resolution and sampling rate) (see Table 2).

Table 2

Comparative analysis of the proposed ADC

Characteristics	Flash ADC	SAR-ADC	Combined ADC
Standard bit number, bits	≤8	≤16	8-14
Maximum frequency, MHz	>1000	<10–100	~10–500
INL, LSB	0.5–1	<0.5	~0.5
DNL, LSB	0.25–1	<0.5	~0.25–0.5
Cost per 1 bit	High	Low	Low/medium
Energy consumption	High	Low	Average

5. Discussion

5.1. Interpretation of the results

The simulation results of the proposed combined analog-to-digital converter indicate its high efficiency in terms of combining accuracy, speed, and implementation cost. In particular, the values of integral nonlinearity (INL) within ±0.5 LSB and differential nonlinearity (DNL) not exceeding ±0.5 LSB confirm the high conversion accuracy characteristic of SAR-ADCs, but at a significantly lower cost than Flash ADCs.

Under the constraint n+m=B (see Eq. 7), the function has an interior minimum; therefore, there exists a pair (n, m) at which

$$E_{conv}(n,m) \le \min\left\{E_{conv}(B,0), E_{conv}(0,B)\right\}$$

Hence, the hybrid ADC configuration's energy consumption does not increase relative to the "pure" flash-only or SAR-only implementations for a fixed B.

The obtained results confirm that the implementation of coarse preliminary conversion using a low-bit Flash ADC allows for preserving the advantage in performance, while the use of the SAR component for further refinement of the difference significantly reduces the overall cost of the device.

5.2. Economic efficiency of the proposed solution

The proposed combined ADC offers a significant reduction in the cost per bit of bit depth compared with traditional Flash ADCs. As demonstrated in the analysis results, the use of Flash ADCs with more than 5 bits results in exponential cost growth, making them inefficient for high bit depth applications. Concurrently, initial SAR ADCs, while low in cost, cannot provide high conversion speeds.

The combined approach, which provides a balanced bit number distribution between the Flash and SAR components, significantly reduces the total cost per bit of bit depth (Fig. 2). The optimal combination is a 4–5-bit Flash ADC and an 8–10-bit SAR ADC, providing the minimum cost per bit of bit resolution.

Additional calculations were performed for the baseline parameters of different ADC architectures. Indicative metrics include the number of comparators, approximate silicon area, and power consumption. An integrated efficiency metric, Cost per MS/s/bit (relative cost normalized to throughput per bit), widely used in specialized literature [1, 16], was also introduced.

Flash ADC, 8-bit - 500 MS/s:
– ~255 comparators;
– die area: approx. 1.5–2.0 mm²;
– power consumption: 300–500 mW;
– Cost per MS/s/bit ≈ 1.5–2.0 (relative units).

SAR ADC, 12-bit - 10 MS/s:
– 1 comparator;
– die area: 0.2–0.3 mm²;
– power consumption: 1–5 mW;
– Cost per MS/s/bit ≈ 0.1–0.2.

Pipeline ADC, 12-bit - 250 MS/s:
– 80–100 comparators with multi-stage operational amplifiers;
– die area: 2.0–2.5 mm²;
– power consumption: 300–500 mW;
– Cost per MS/s/bit ≈ 1.0–1.3.

Proposed combined ADC (Flash 4–5 bits + SAR 8–10 bits), 100–200 MS/s:
– 15–31 comparators;
– die area: 0.6–0.8 mm²;
– power consumption: 50–80 mW;
– Cost per MS/s/bit ≈ 0.4–0.6.

Therefore, within the medium-speed range (100–250 MS/s), the proposed combined architecture achieves a 30–40% reduction in cost per bit and a 2–3× reduction in power consumption compared to pipeline ADCs, while maintaining comparable throughput.

This approach makes the proposed architecture particularly attractive for the mass production of analog-to-digital converters used in industry, communication systems, and portable devices, where cost is a key factor alongside speed and accuracy.

All presented data were derived from reference manuals and official sources and should be regarded as theoretical estimates. This limitation arises because Ukraine currently lacks a developed manufacturing base for the large-scale production of state-of-the-art ADCs. Practical parameters may vary and would need to be verified during actual design and fabrication.

5.3. Potential areas for enhancement

The proposed combined architecture has significant potential for further development and improvement. The main directions for future research include the following:

– **optimization of the component base**: selection of more efficient analog comparators and improvement to the digital-to-analog converter architecture will further reduce conversion deviations and lower power consumption;

– **analysis of the impact of noise and component deviations:** further research may include studying the effects of real noise and deviation in comparators and DACs on the combined ADC performance, which would allow for the development of recommendations to compensate for these deviations;

– **implementation of an adaptive bit allocation system:** the development of adaptive algorithms that automatically adjust the ratio of Flash and SAR components according to operating conditions, input signal characteristics, and conversion speed and accuracy requirements represents a promising area of research;

– **experimental testing of real devices:** The creation of an experimental sample of the proposed ADC with further measurements of real-world technical characteristics is a significant area for future research. This will serve to confirm and refine the theoretical conclusions.

Consequently, the findings of this study provide a foundation for the subsequent development and practical implementation of new generation combined analog-to-digital converters that optimally combine speed and efficiency.

6. Conclusions

This study proposes a combined architecture for an analog-to-digital converter, which integrates a low-bit depth Flash ADC for rapid coarse conversion and a successive approximation register ADC for precise refinement of the residual difference. The obtained results lead to the following key conclusions:

1. The proposed combined approach represents an effective compromise between Flash ADCs' high performance and SAR ADCs' cost-effectiveness. A significant reduction in the number of comparators results in substantial cost savings per bit of bit depth.

2. The analysis of economic indicators demonstrated that the balanced combination for a contemporary element base is a Flash ADC with a bit depth of 4-5 bits and a SAR ADC with a bit number of 8-10 bits. This combination provides minimal cost per bit with high overall conversion accuracy.

3. The simulation results confirmed the high accuracy and stability of the proposed combined ADC. The integral nonlinearity (INL) and differential nonlinearity (DNL) values were found to be no greater than ±0.5 LSB, indicating that the proposed architecture meets contemporary accuracy requirements.

4. A comparative analysis with existing types of ADCs was conducted, which demonstrated the combined solution's advantage. This solution was found to be significantly more cost-effective than Flash ADCs and outperform SAR ADCs of similar bit depth.

5. Potential directions for future research are delineated, encompassing the analysis of the impact of real noise and deviations, in addition to the fabrication of experimental device prototypes, which will further substantiate the proposed architecture's practical efficiency.

Thus, the proposed combined ADC architecture is of high practical significance and can be effectively used in systems where achieving an optimal balance between cost, speed, and conversion accuracy is critical.

Contributions of authors: conceptualization, methodology – **Oleksiy Azarov**; formulation of tasks, analysis – **Maksym Obertiukh**; development of model, software verification – **Oleksandr Dudnyk**; analysis of results, visualization – **Oleksandr Lukashuk**; writing – original draft preparation, writing – review and editing – **Oleksandr Murashchenko**.

Conflict of Interest

The authors declare that they have no conflict of interest in relation to this research, whether financial, personal, authorship or otherwise, that could affect the research and its results presented in this paper.

Financing

This study was conducted without financial support.

Data Availability

The work data will be made available upon reasonable request,

Use of Artificial Intelligence

The authors have used artificial intelligence technologies within acceptable limits to provide their own verified data, which is described in the research methodology section.

ISSN 1814-4225 (print)
ISSN 2663-2012 (online)

All the authors have read and agreed to the published version of the manuscript.

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Received 17.03.2025, Received in revised form 10.10.2025
Accepted date 17.11.2025, Published date 08.12.2025

КОМБІНОВАНА АРХІТЕКТУРА АНАЛОГО-ЦИФРОВОГО ПЕРЕТВОРЮВАЧА ЗІ ЗБАЛАНСОВАНИМ СПІВВІДНОШЕННЯМ ШВИДКОДІЇ ТА ВАРТОСТІ

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Предметом вивчення в статті є комбінована архітектура аналогово-цифрового перетворювача (АЦП), яка базується на поєднанні флеш-АЦП невеликої розрядності та АЦП порозрядного врівноваження (SAR-АЦП). Флеш-АЦП характеризується високою швидкодією, проте має суттєвий недолік, пов'язаний з експоненційним зростанням вартості на одиницю біта роздільної здатності зі збільшенням розрядності, тоді як SAR-АЦП вирізняється низькою вартістю, проте має обмежену швидкість перетворення через послідовний принцип роботи. **Метою** статті є дослідження можливості створення комбінованої архітектури АЦП, що дозволяє збалансовано поєднати переваги флеш та SAR-перетворювачів, забезпечуючи при цьому максимальну економічну ефективність на одиницю біта роздільної здатності. Основна гіпотеза полягає в тому, що використання флеш-АЦП невеликої розрядності для первинного швидкого перетворення сигналу та SAR-АЦП для точного доопрацювання залишкового сигналу дозволить суттєво зменшити витрати на реалізацію високорозрядних АЦП. **Завдання**: провести аналіз характеристик флеш та SAR-АЦП, розробити алгоритм роботи комбінованого АЦП, визначити збалансовану комбінацію розрядноtей такого АЦП, створити його математичну модель у середовищі MATLAB Simulink, та здійснити оцінку його техніко-економічних показників. Отримані результати статті показують, що комбінація флеш-АЦП з розрядністю 4–5 біт та SAR-АЦП із розрядністю 8–10 біт дозволяє значно знизити витрати на одиницю біта роздільної здатності порівняно з традиційними флеш-структурами, при цьому зберігаючи значно вищу швидкодію порівняно з SAR-АЦП аналогічної розрядності. В результаті моделювання було встановлено, що інтегральна (INL) та диференціальна (DNL) нелінійності запропонованого АЦП не перевищують ±0,5 LSB, що свідчить про високу точність перетворення. Додатково показано, що запропонована комбінація не призводить до збільшення споживаної енергії на перетворення порівняно з чистими flash/SAR підходами. Крім того, аналіз економічних характеристик доводить, що запропонований підхід забезпечує мінімальні витрати при заданій роздільній здатності. **Висновки**. Запропонована комбінована архітектура АЦП демонструє суттєві переваги за критерієм економічної ефективності порівняно із класичними флеш-АЦП та забезпечує значне покращення швидкодії у порівнянні з SAR-АЦП. Встановлено, що існує співвідношення розрядностей флеш- та SAR-компонентів яке дозволяє ефективно збалансувати економічні та технічні вимоги до пристрою. Подальші дослідження мають бути зосереджені на практичній реалізації запропонованого рішення, аналізі впливу шумів та адаптивному керуванні розрядностями АЦП.

Ключові слова: аналогово-цифровий перетворювач; флеш-АЦП; SAR-АЦП; комбінована архітектура; енергоефективність; вартість на 1 біт; нелінійність.

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