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HYPER REDUNDANCY FOR SUPER RELIABLE FPGAs

*The **subject** of the research presented in the article is hyper-redundant elements and FPGA devices that can be used in highly reliable digital systems (HRDS). The current work develops hyper-reliable logic elements, memory elements, and buffer elements for HRDS based on FPGAs, their simulation, and reliability assessment. **Objective:** to develop fault-tolerant logical elements of LUT for one, two, and three variables. Develop fault-tolerant static random access memory, D – flip-flop, and buffer element. To do a simulation in NI Multisim to validate performance and estimate complexity and power consumption. Derive formulas for assessing the reliability of the developed elements and devices and build graphs of comparison with known methods of triple modular redundancy. **Methods** used the introduction of redundancy in transistor level, simulation methods in Multisim, mathematical estimations of transistor number, reliability calculations. The following **results** were obtained: when introducing redundancy at the transistor level and using series-parallel circuits, it is necessary to at least quadruple the number of transistors. Passive-fail-safe elements and devices have been developed that can withstand one, two, and three transistor failures (errors). An assessment of their effectiveness has been conducted, showing their preference over the majority reservation. **Conclusions**. The synthesis and analysis of passive-fault-tolerant circuits with an ocean of redundancy, which ensures the preservation of a logical function for a given number of failures (from one to three), have been conducted. The costs are more than to maintain functional completeness in the method previously proposed by the author, but they are worth it. Despite the significantly greater redundancy compared to majority redundancy, power consumption turned out to be lower with an insignificant increase in latency. The proposed hyper-fault-tolerant FPGAs are advisable to use in critical application systems when maintenance is impossible. In the future, it is advisable to consider the issue of redundancy at the transistor level using bridge circuits.*

***Keywords:** LUT; Passive Fault-Tolerant Systems; Reliability; Redundancy.*

Introduction

Motivation. Highly reliable systems beginning Shannon, Von Neumann [1] and Avizienis articles [2] are one of the current areas of modern technology [3, 4]. For example, these are medical systems, military systems, control of nuclear power plants [5], aerospace systems. They are include Radiation Hardened by Design too [6-8]. Fault-Tolerant Systems (FTS) uses of structural, temporal or information redundancy to ensure the reliability. Passive FTS (PFTS) due to a very large redundancy (Modular Redundancy) produces fault masking [9]. An Active Fault-Tolerant Systems (AFTS) have less redundancy, but requires comparatively more diagnostic and reconfiguration time to switch out faulty elements and to switch in spare elements [9]. Deep Triple Modular Redundancy (TMR), i.e. k-layer TMR has a depth to single gate. Transistors cannot be tripled, although redundancy at the transistor level allows you to reach the very high Reliability, which can be called "Ocean of the Redundancy" [10]. Such redundancy is a variant of the so-called functionally complete tolerant elements [11], when the original logical function is preserved [12].

State of the art. FPGAs [13] are the most general element of the modern digital equipment in general and the base of the SoC (System-on-Chip), SiP (System-in-Package) in particular [14-16]. Impressive progress has been achieved in the field of logic implementation, the number of logic elements reaches tens of millions [17], new efficient Tri-Gate transistors have been created [18,19] and provide a completely new level of efficiency, including reliability. Despite the fact that FPGAs are vulnerable to radiation due to the large amount of RAM, they are used in highly reliable systems, for example, in Mars rovers. Triple Modular Redundancy is already used in re-programmable FPGAs [20]. FPGA-based instrumentation and control systems Safety Platform for Nuclear Power Plants, for example, represented [21]. FPGA Technology for the Multi-Version Safety described publication [22]. However, a qualitative leap in reliability has not happened, although he has already matured. It should be a multi-layered reliability system,

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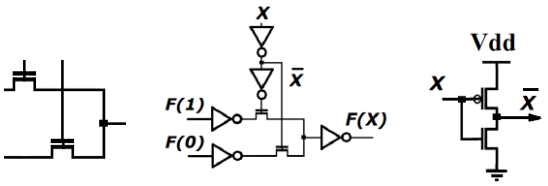
in which redundancy begins at the nanoscale [10-12]. **Goal and structure.** To design and investigate base FPGA's elements – LUTs (Look up Table), NOT gate, SRAM cell, Flip-Flop, 3-State Buffer with the redundancy at the transistor level. To compare the proposed solutions with tripling.

The structure of the article includes an analysis of the existing LUTs, the development of a fault-tolerant NOT gate, LUTs for one, two and three variables. Then author investigates Fault Tolerant Memory (RS Flip-Flop, SRAM, D Flip-Flop) and Buffers. The article performs simulation and evaluation of the PFT FPGA's elements for the Hyper Reliable Systems (HRS) with "Ocean of the Redundancy" which may mark a new stage of FTS development following the "Sea of Gates" [23].

LUT

LUT (Look up Table or Truth Table or Functional Generator) for the n variables how the base of a FPGA logic [24, 25] is a multiplexer (MUX) 2^n-1, which in other words is $2^{n+1}-2=2\cdot(2^n-1)$ n-MOS pass–transistor's tree. For example at n=1 we have – Fig.1



a) b) c)

Figure 1. LUT-1: a) p-MOS pass transistor's tree 2^1 – MUX 2-1; b) *F(0), F(1)* – masks from configurations memory (CRAM); c) CMOS NOT Gate

The SRAM cells for storage *F(0), F(1)* themselves are not shown in Fig.1 Connecting two MUX 2-1 trees by third MUX 2-1 tree, we get LUT-2, as shown Fig. 2.

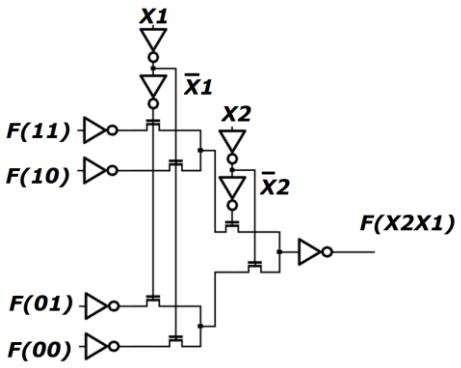


Figure 2. LUT-2; $F(00)_2$, $F(01)_2$, $F(10)_2$, $F(11)_2$ – CRAM masks

So we can set any from the $2^{2^1}=4$ functions $F(X2X1)$ having four bit Configuration Read Only Memory (CRAM) $F(00)_2$, $F(01)_2$, $F(10)_2$, $F(11)_2$. Similarly, we can get LUT-3 for $F(X3X2X1)$ (Fig. 3).

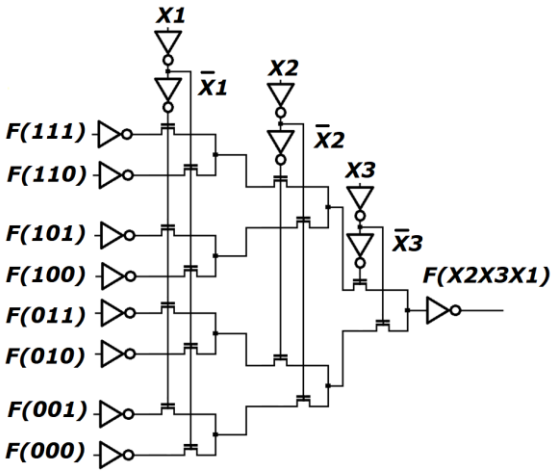


Figure 3. LUT-3;
$F(000)_2$, … $F(111)_2$ – CRAM masks

But LUT-4 for $F(X4X3X2X1)$ according Mead-Conway rules [26] must include additional invertors (signal's level restorations blocks) and, of course, additional MUX 2-1 – Fig. 4.

Therefore, LUT-3 is the base block of the FPGAs logic. The complexity of LUT-n in the number of transistors with n <= 4 can be estimated by the expression (1):

$$L_n = 2^n\cdot 8+2^{n+1}+4n. \qquad (1)$$

Decomposing LUT-n an n-tree with k LUT, $k\in\{1, 2, 3, 4\}$, $8 <= n > = k$, we get:

$$L_{n.k} = 2^n\cdot 8+(2^{k+1}+2k)\cdot 2^{n-k}+ +(2^{2^{n-k}}+1+2^{n-k+1})+4n. \qquad (2)$$

The obtained estimates can be used for the LUT-n reliability calculating.

Fault Tolerant LUT

Using Quadded transistors in CMOS NOT Gates, SRAM cells and in pass transistors, we obtain proposed Fault Tolerant LUT-1 – Fig. 5. Every transistor is redundant! We have in fact functional complete tolerant [11] expression $xx\vee xx$ for n-CMOS transistors (else variant $[x\vee x][x\vee x]$). Similarly for p-CMOS transistors NOT gates we can get $\bar{x}\bar{x}\vee\bar{x}\bar{x}$ and $[\bar{x}\vee\bar{x}][\bar{x}\vee\bar{x}]$.

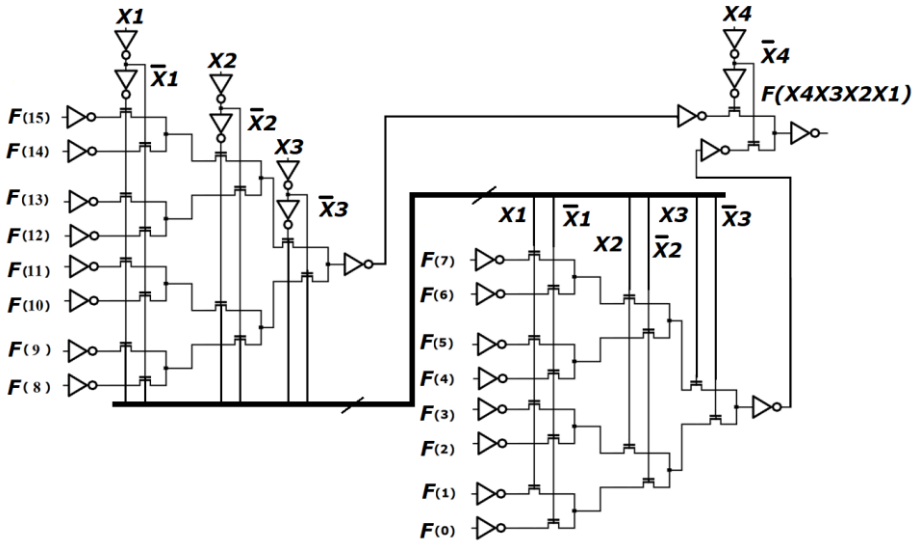


Figure 4. LUT-4; *F*(0), … *F*(15) – CRAM masks

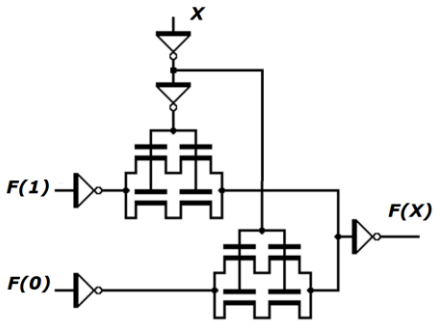


Figure 5. Fault Tolerant LUT-1T

Any failure of any (only single) of the four transistors will not cause the entire group to fail. For example: $x\bar{x} \vee 1x = x; 0x \vee xx = x; x\bar{x} \vee xx = x$.

It is hyper reliability! The same redundancy is used in inverters (inside NOT gates). The time delay is doubled (the signal passes two transistors instead of one). Following this principle, we get LUT-2T, in which four transistors in a row – Fig. 6.

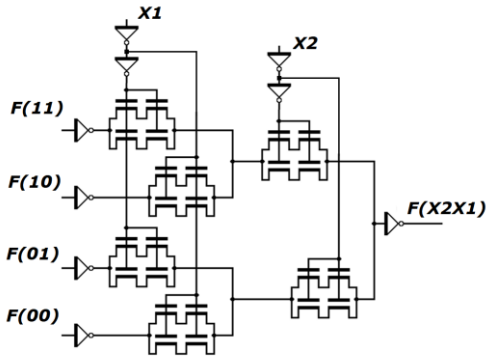


Figure 6. Proposed Fault Tolerant LUT-2T

Therefore, to implement LUT-3T, signal buffering is required by introducing additional recovery inverters – Fig. 7.

Thus (Fig. 5-7), for parrying the failure of one transistor in each group of the four transistors necessary four-fold redundancy. To parry the failures of any two transistors, nine-fold redundancy is necessary. Fig. 8 shows Fault Tolerant LUT-1T2.

However, the time delay is tripled. Fig. 9 shows Fault Tolerant LUT-1T3.

The time delay is quadrupled. It should be noted that such redundancy is similar in other elements of LUT (inverters –NOT gates and SRAM cells).

Further increasing of the redundancy violates the rules of Mead-Conway. It should be noted that such restrictions might be relaxed by using Tri-Gate transistors.

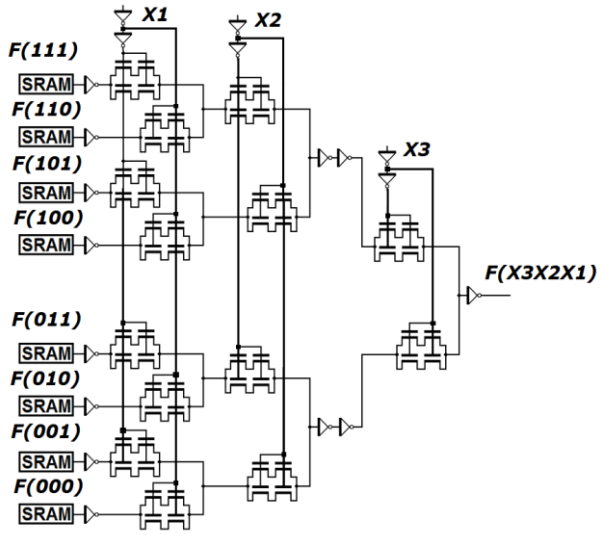


Figure 7. Fault Tolerant LUT-3T

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For example on Fig. 8: $xxx \vee xxx \vee 10x = x$.

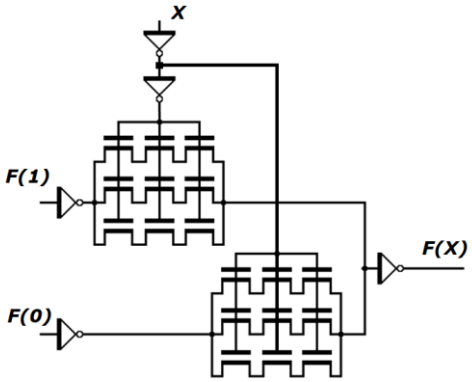


Figure 8. Fault Tolerant LUT-1T2
(expression $xxx \vee xxx \vee xxx$ masks any failures
of any two transistors)

For example on Fig. 9: $xxxx \vee xxxx \vee xxxx \vee 101x = x$. Using LUT-1T2, LUT-1T3 we can designed LUT-2T2, LUT-2T3, LUT-3T2, LUT-3T3.

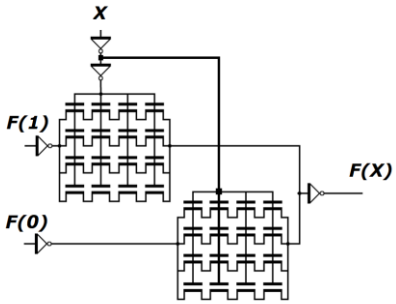


Figure 9. Fault Tolerant LUT-1T3
(expression $xxxx \vee xxxx \vee xxxx \vee xxxx$ masks
any failures of any three transistors)

Fault Tolerant Memory and Buffers

Configurations memory (CRAM) contains six-transistor SRAM cells – Fig. 10.

It is obvious that the restrictions of the Mead-Conway with the introduction of redundancy at the transistor level are observed. Each transistor of the SRAM cell (Fig. 10) is reserved accordantly Fig. 5. Analysis D Flip-Flop allows you to set the applicability of the above-described reservation – Fig. 11.

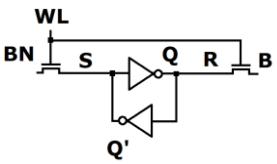


Figure 10. SRAM cell, B (R – reset),
BN (S – set) – bit lines; WL – write line;
Q, Q' – outputs

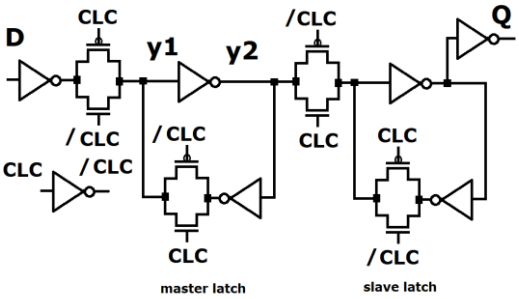


Figure 11. D Flip-Flop, "Master-Slave" latch;
CLC – clock inputs; D – date input

Similarly, one can make sure that the Mead-Conway rules are observed and with the introduction redundancy to the buffer – Fig. 12.

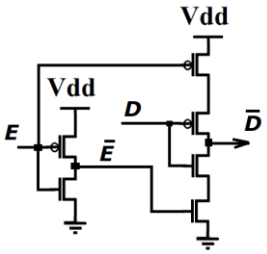


Figure 12. 3-state buffer:
E – enable input; D – data input

Similar technologies can be used to increase the reliability of connections in the FPGA, which are in many ways similar to LUT. Thus, the proposed redundancy can be implemented in all basic elements and devices of the FPGA.

Fault Tolerant Elements Simulation

Circuit simulation is performed to confirm operability and assess current consumption and delay in the system NI Multisim (National Instruments Electronics Workbench Group). Dynamic and static models of the Invertor (CMOS NOT gate) with transistors redundancy (ideal model of the transistors), parrying any fault of the transistors, shows Fig. 13. In static proposed NOT gate perform true calculation: $x = 1, F(x) = 0$ (Fig. 13, a); $x = 0, F(x) = 1$ (Fig. 13, b). In dynamic waveform (Fig. 13, c) is correct, but the performance is slightly reduced, then of the usual NOT gate with two transistors (Fig. 1, c).

Proposed MUX 2-1 of the LUT-1T (free available Spice Model BSIM4.8, 65nm) shows Fig. 14, a. Q1,Q2,Q3,Q4 are the quadrupled transistor Q for the X input (Fig. 1, a), Q5,Q6,Q7,Q8 are the quadrupled transistor Q for the not X input (Fig. 1, a). Sram0, sram1

are the masks from configurations memory *F*(0), *F*(1) (Fig. 1, b). Out 0 (Fig. 14, a) – is the *F(x)* (Fig. 1, b). NOT Gate is not shown. Such quadrupled LUT-1 is compared with Triple Modular Redundancy LUT-1 (Fig. 14, b). ME – is Majority Voter, Majority Element with function $x_1x_2 \vee x_1x_3 \vee x_2x_3$, x_1, x_2, x_3 - outputs of the channels LUT1, LUT2, LUT3.

A comparison of the power consumption of the LUT-1T/LUT-1 TMR at 1 V Power Supply shows Fig. 14, c). Despite the larger number of transistors, LUT QR (Fig. 14, a) wins LUT TMR in power consumption, although one non-redundant LUT consumes significantly less than LUT TMR, LUT QR. Similar results were obtained for other supply voltages in range 0,2…5 V. Layout simulation in MicroWind (free version) also confirmed the results obtained in the system NI Multisim.

Fault Tolerant 3-State Buffer Simulation shows Fig. 15. Each transistor shown in Fig. 12 is quadrupled: NOT gate is consist of four p-MOS transistors and four n-MOS transistors (fault tolerant NOT gate on the Fig. 15). Data transistors are two n-MOS transistors 1,2 and two p-MOS transistors 3,4. Faults simulation is similar Fig.13 b.

Quad CMOS SRAM cell simulation shows Fig. 16. Proposed Fault tolerant SRAM cell has two Fault tolerant NOT gates1,2 (outputs Q,Q' on the Fig. 10) and two control n-MOS Fault tolerant transistors 1,2 (B,BN on the Fig.10). Faults simulation has confirmed the effectiveness of the proposed cell in comparison, for example, with DICE SRAM [7].

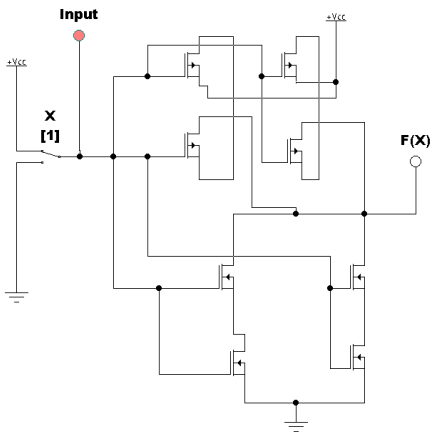
D Flip-Flop Simulation (Master block) shows Fig. 17. Each transistor shown in Fig. 17 is quadrupled too. The Slave block was simulated similarly.

Therefore, simulation confirms the correct operation of the FPGAs elements with "Ocean of the redundancy".

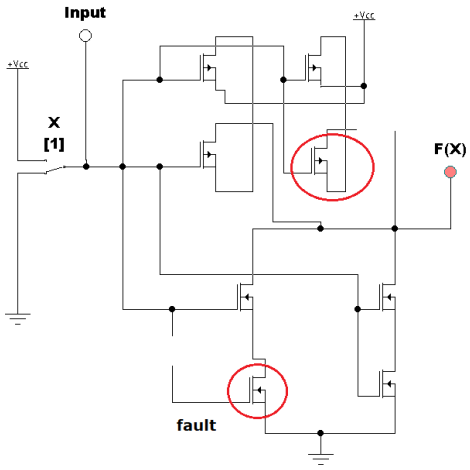
The proposed redundancy reduces performance and can be used at the level of individual devices, and maybe at the level of the entire FPGA, to arbitrate other, faster, but not redundant at the transistor level, devices. Hybrid redundancy is possible, for example, transistor redundancy is used for configuration RAM, as the least speed-critical FPGA device, and the rest of the blocks are tripled. It also makes sense to investigate such redundancy for buffer elements, and use channel-by-channel redundancy for memory and logic elements.

Fault Tolerant Elements Evaluation

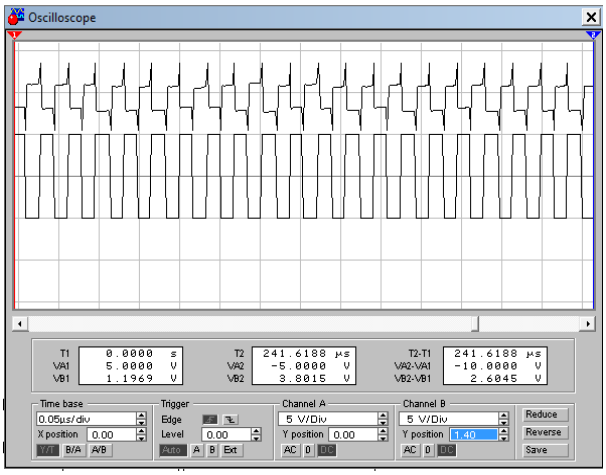
Redundancy on the transistors level does not required Majority Voters, so we can get parrying, for example, any fault of one transistors from four transistors for the each transistors – expression 3 (Weibull distribution [27]):



a)



b)



c)

Figure 13. CMOS NOT gate with transistors redundancy simulation: a) x=1; F(x)=0; b) x=0; F(x)=1 at the faults of the transistors, which dedicated red rings; c) waveform of the dynamic simulation

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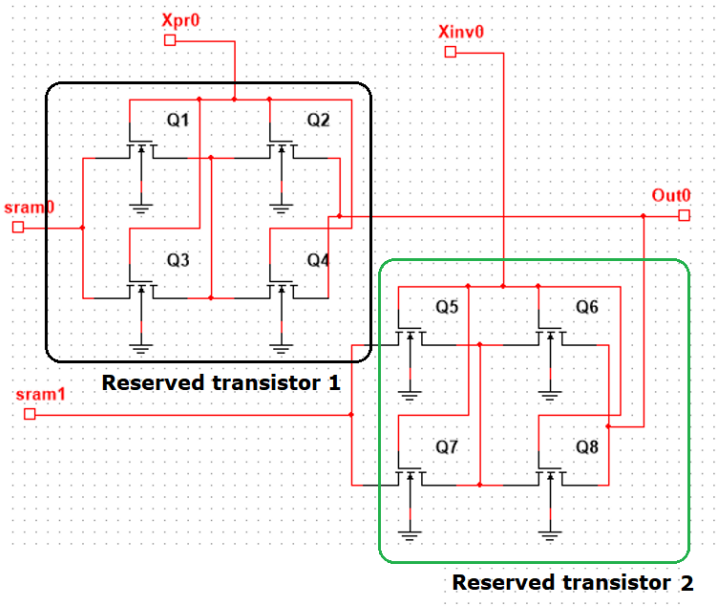
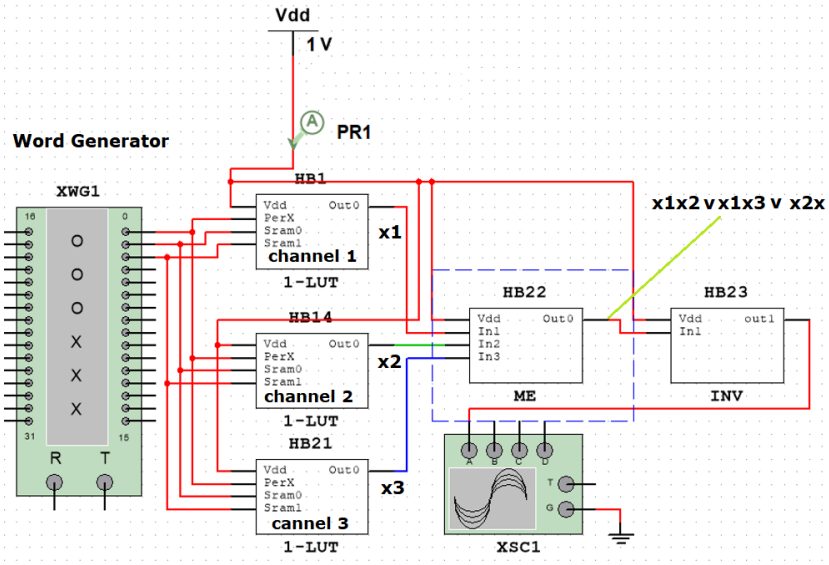


a)



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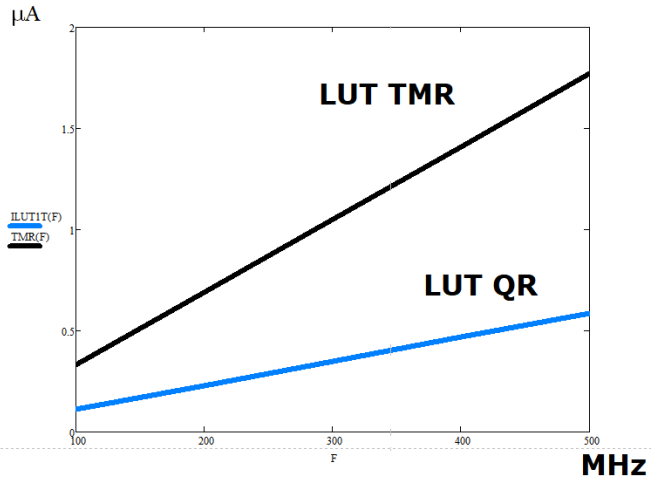

c)

Figure 14. Simulation of the LUT FPGA (n=1): a) LUT-1T; b) LUT -1 TMR;
c) a comparison current of the LUT-1T – LUT QR (Quad Redundancy Fig. 5),
LUT-1 TMR – LUT TMR at 1 V Power Supply

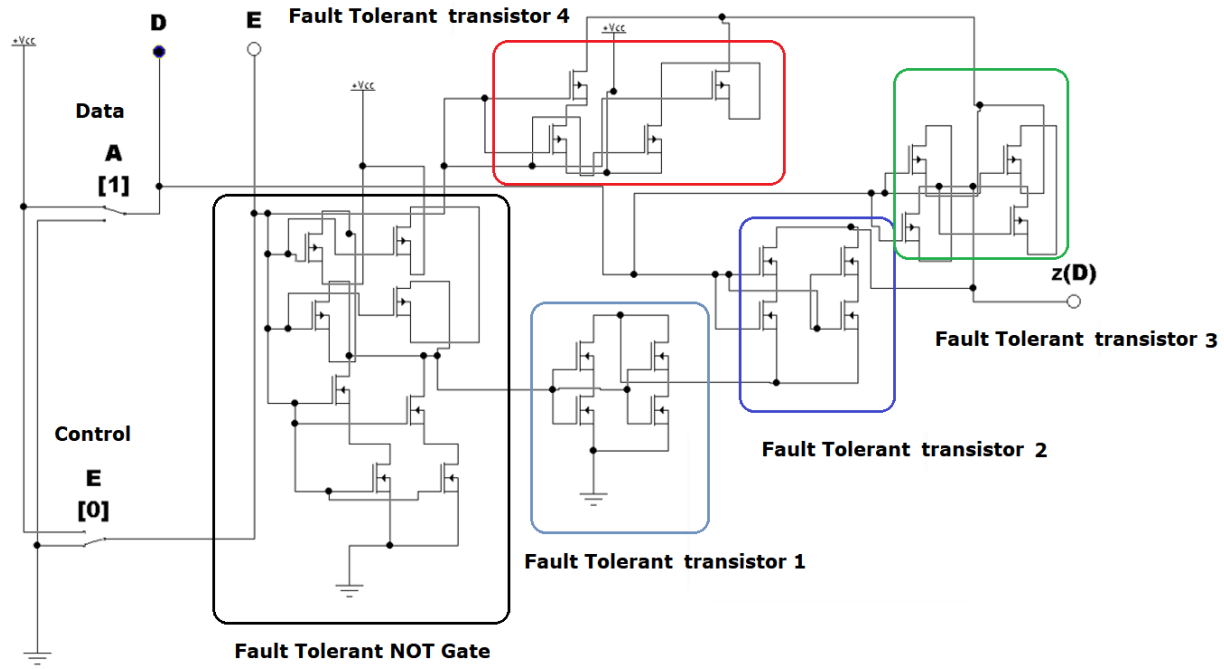

Figure 15. Fault Tolerant 3-State Buffer Simulation

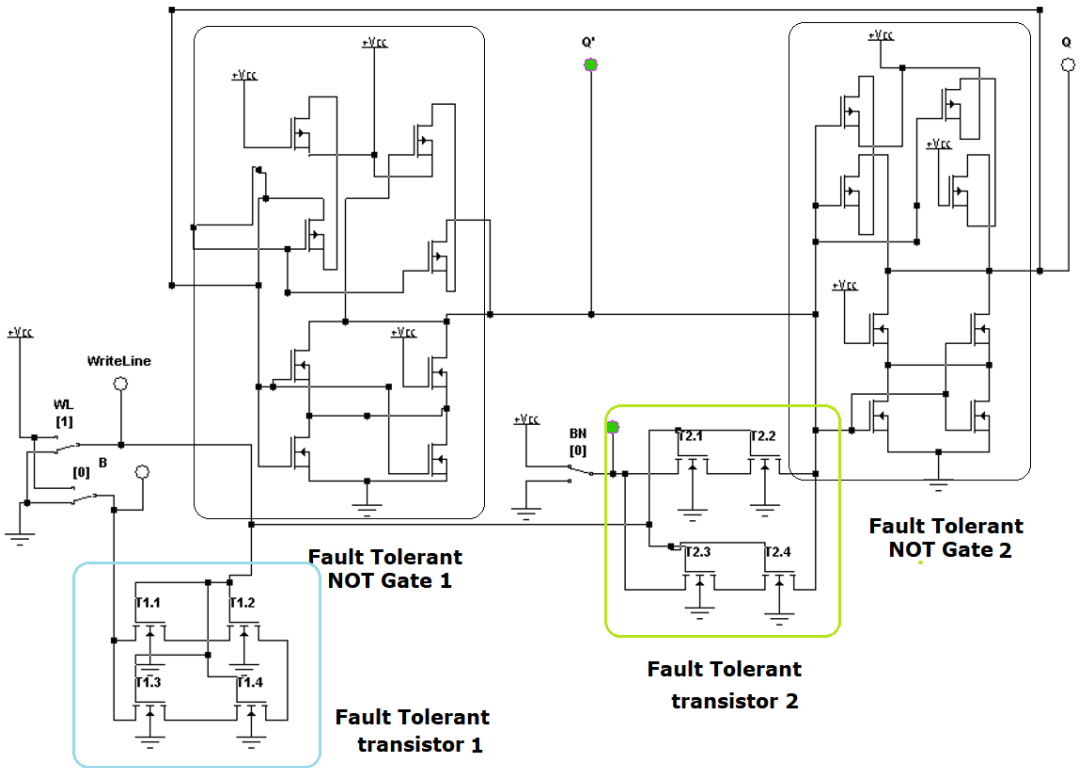

Figure 16. Quad CMOS SRAM cell simulation

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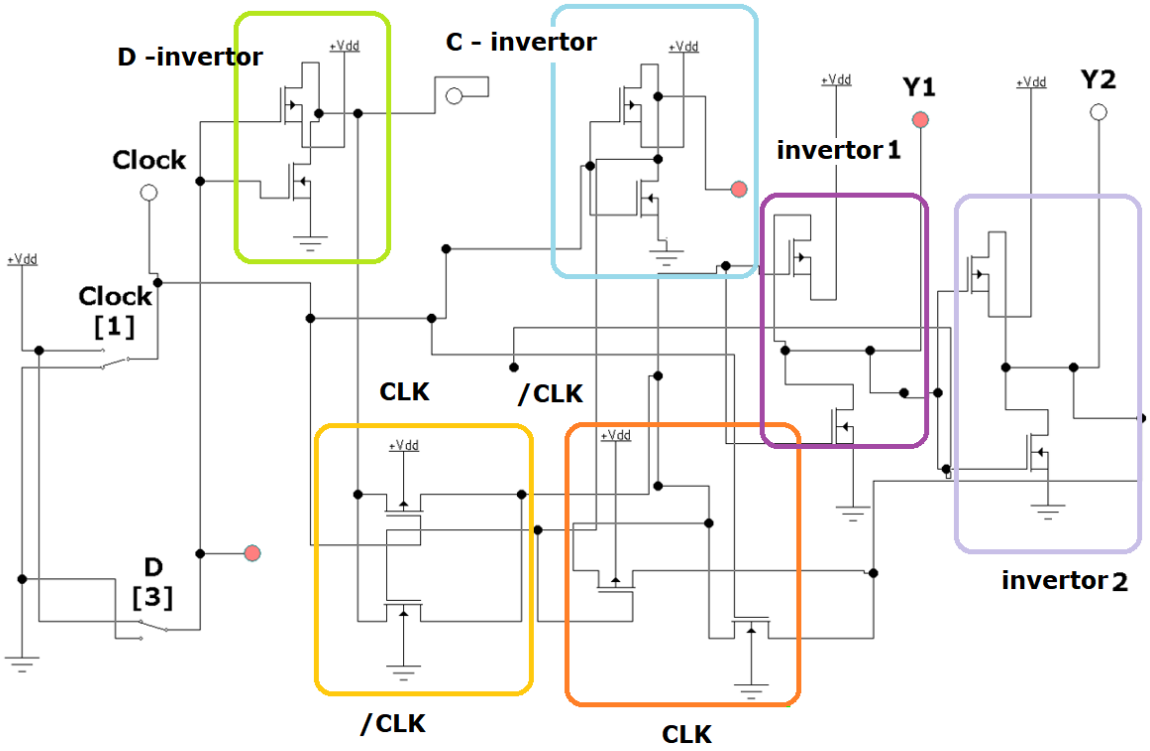

Figure 17. D Flip-Flop Simulation (Master block), Y1, Y2 – outputs, shown Fig.11

$$P(t)_{ft1} = [e^{-4\cdot\lambda\cdot t^{\alpha}} + 4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}} \cdot (1-e^{-\lambda\cdot t^{\alpha}})]^{n}, \quad (3)$$

where n – is a complexity of the device in amount of the transistors, α is a Weibull distribution coefficient $1 \le \alpha \le 2$; λ is a failure rate of one transistor (1/hour), t – is an operation time in hours.

In common case parrying any faults one of the transistors from $(v)\ from\ (v+1)^2$ we get formula (4)

$$P_{n/(v)\ from\ (v+1)^2}(t) = [\sum_{i=0}^{v} C^{i}_{(e+1)^2} \{e^{-[(e+1)^2 - i]\cdot\lambda\cdot t^{\alpha}} \cdot (1-e^{-\lambda\cdot t^{\alpha}})^{i}\}]^{n}. \quad (4)$$

Failure-free operation probability of the usual Triple Modular Redundancy system is described by expression (5):

$$P_3 = (3\cdot e^{-2\cdot(n)\cdot\lambda\cdot t^{\alpha}} - 2\cdot e^{-3\cdot(n)\cdot\lambda\cdot t^{\alpha}})\cdot e^{-(12)\cdot\lambda\cdot t^{\alpha}}. \quad (5)$$

This method is parrying only one fault in one of the three channels (or one of the power supply). Note that "12" is a complexity of the Majority Vote Circuit in amount of the transistors. With the Majority Voters tripling, we get formula (6):

$$P_{33} = (3\cdot e^{-2\cdot(n)\cdot\lambda\cdot t^{\alpha}} - 2\cdot e^{-3\cdot(n)\cdot\lambda\cdot t^{\alpha}})\cdot (3\cdot e^{-2\cdot(12)\cdot\lambda\cdot t^{\alpha}} - 2\cdot e^{-3\cdot(12)\cdot\lambda\cdot t^{\alpha}}). \quad (6)$$

In this case is parrying of the failure in one of the three channels and in one of the Majority Voters (or one of the power supply too).

Then we can get from (4) formula (7) to parrying any three faults in sixteen transistors (v=2) – expression 7

$$P(t)_{ft2} = e^{-(9)\cdot\lambda\cdot t^{\alpha}} + 9\cdot e^{-8\cdot\lambda\cdot t^{\alpha}}(1-e^{-1\cdot\lambda\cdot t^{\alpha}}) + 36\cdot e^{-7\cdot\lambda\cdot t^{\alpha}}(1-e^{-1\cdot\lambda\cdot t^{\alpha}})^2. \quad (7)$$

We can get from (4) parrying any three faults in sixteen transistors (v=2) – expression 8

$$P(t)_{ft3} = e^{-(16)\cdot\lambda\cdot t^{\alpha}} + 16\cdot e^{-15\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}}) + 120\cdot e^{-14\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})^2 + 560\cdot e^{-13\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})^3. \quad (8)$$

A further increase in redundancy leads to a violation of the existing of the Mead-Conway rules, so we will not consider them. Let the failure-free operation probability of the n-transistors device equal $e^{-n\cdot\lambda\cdot t^{\alpha}}$. Failure-free operation probability curves (3), (5), (6) for different *n* shows Fig. 18. Calculations show the best failure-free operation probability of the proposed devices $Pft1(t)$ (green lines, v=1) compared to the original circuit $e^{-\lambda\cdot t^{\alpha}}$ (red line) and tripling $P(t)_3$ (blue line) $P(t)_{33}$ (black line). With a small number of transistors, triplication is impractical – Fig. 18, a,b.

Failure-free operation probability curves (3), (5) - (8) for different *n*) in the range of the probability 0.1-1 shows Fig. 19. We observe the best values $Pft1(t)$ (green line), $Pft2(t)$ (purple line), $Pft3(t)$ (light blue line) over the entire range of probabilities, as opposed to tripling – Fig. 19, a, b, c. It should be borne in mind that passive fault tolerance is considered here, therefore the time interval is relatively short (to 200 hours), and the failure rate is very high (10^{-5} 1/h), which corresponds to critical applications operating in harsh environments.

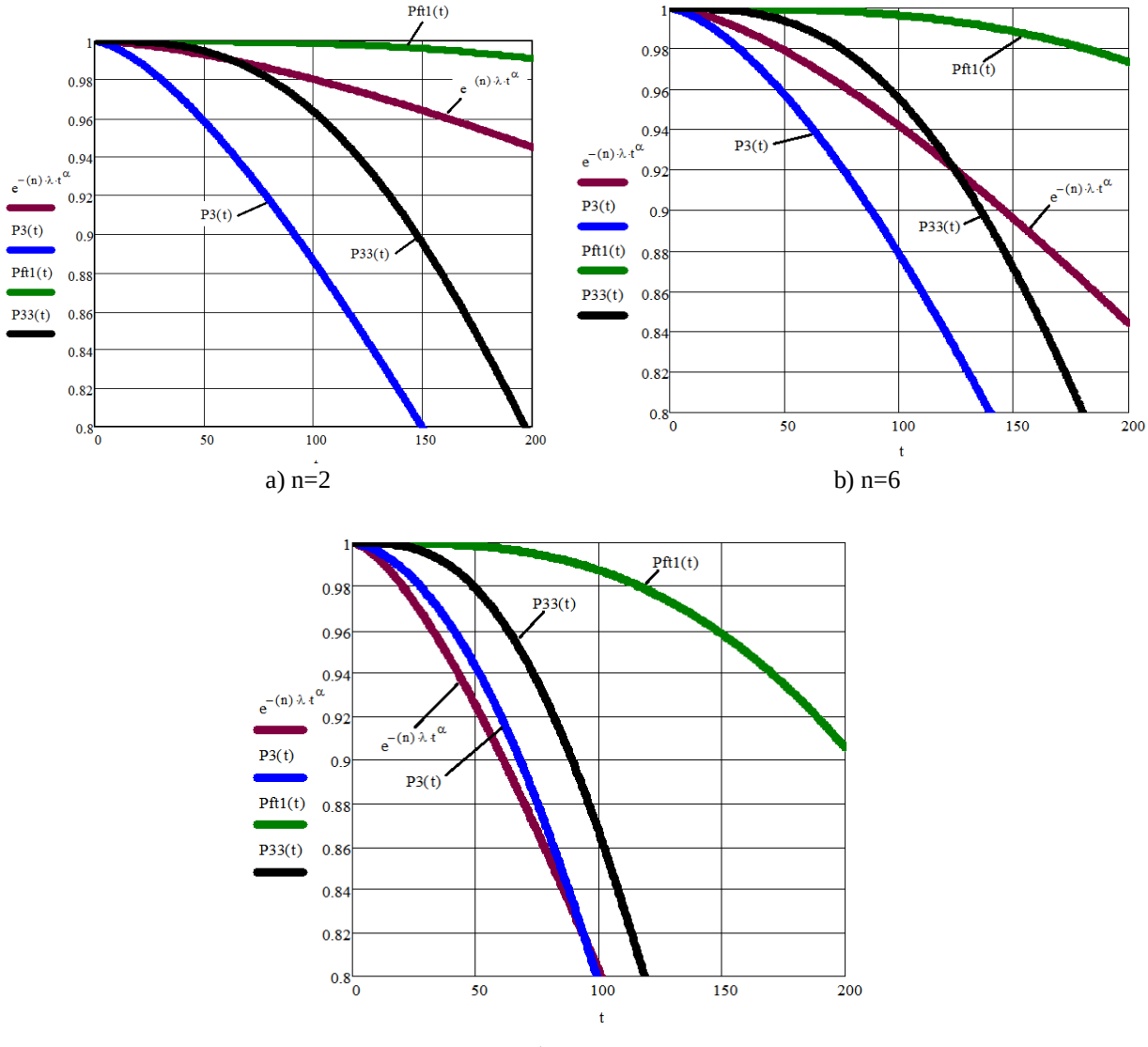

Figure 18. Failure-free operation probability curves of the n-transistors device $e^{-\lambda\cdot t^{\alpha}}$, device with TMR $P(t)_{33}$, $P(t)_3$, device with "Ocean of the Redundancy" $Pft1(t)$; ($\alpha = 1{,}5; \lambda = 10^{-5}$): a) n=2 (CMOS NOT gate); b) n=6 (SRAM cell, 3-state buffer); c) n=22 (D-Flip-Flop)

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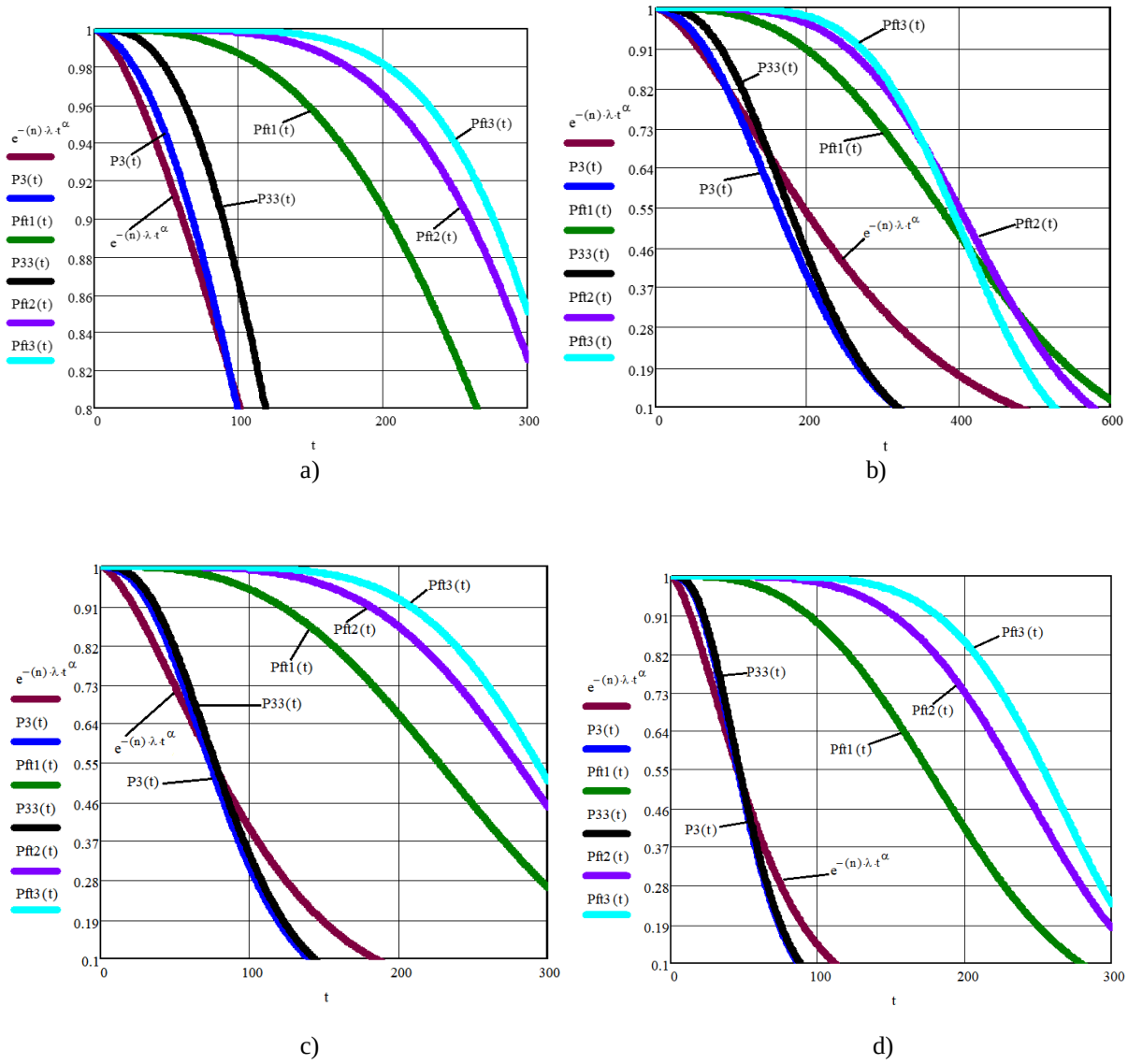

Figure 19. Failure-free operation probability curves of the n-transistors device $e^{-\lambda \cdot t^{\alpha}}$, device with TMR $P(t)_3$ $P(t)_{33}$, device with "Ocean of the Redundancy" $P(t)_{ft1}$, $P(t)_{ft2}$, $P(t)_{ft3}$ ($\alpha = 1{,}5; \lambda = 10^{-5}$): a) n=22 (SRAM cell, 3-state buffer) in the range of the probability 0.8-1; b) n=22 (SRAM cell, 3-state buffer) in the range of the probability 0.1-1; c) n=92 (LUT-3) with SRAM cells; d) n=188; LUT-4 with SRAM cells

Conclusion

Therefore, the "Ocean of the Redundancy" allows you to get a higher failure-free operation probability than tripling (TMR), and over the entire time range. To parry any one fault in each transistor structure, fourfold redundancy is necessary. Ninefold redundancy is needed to achieve a more substantial probability of failure-free operation. An even bigger effect is given by the structure, which parries the failures of any three transistors, but it requires sixteen times redundancy. Design of the "Ocean of the Redundancy" systems must be take into account the necessary hardware costs and time delay.

It is also possible to additionally reserve transistor connections and duplicate the power supply. This approach can also be applied at the level of neural networks, which requires additional research. A comparison of the devices "Ocean of the Redundancy" and modular redundancy devices shows the preference first for energy consumption. In the future, we should consider redundancy directly in the topology of one transistor.

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ГИПЕРИЗБЫТОЧНОСТЬ ДЛЯ СВЕРХНАДЕЖНЫХ ПЛИС

С. Ф. Тюрин

Предметом исследования, представленного в статье, являются гиперизбыточные элементы и устройства ПЛИС, которые могут быть использованы в высоконадежных цифровых системах (ВНЦС). **Целью** данной работы является разработка гипернадёжных логических элементов, элементов памяти, буферных элементов для ВНЦС на основе ПЛИС, их моделирование и оценка надежности. **Задача**: разработать отказоустойчивые логические элементы LUT на одну, две и три переменные. Разработать отказоустойчивую статическую оперативную память, Д-триггер и буферный элемент. Выполнить симуляцию в NI Multisim для подтверждения работоспособности и оценки сложности и потребляемой мощности. Вывести формулы для оценки надёжности разработанных элементов и устройств и построить графики сравнения с известными методами троирования. Используемые **методы**: введение избыточности на уровне транзисторов, методы моделирования в Multisim, математические оценки количества транзисторов, расчеты надежности. Были получены следующие **результаты:** при резервировании логики на транзисторном уровне и использовании последовательно-параллельных цепей необходимо минимум учетверение количества транзисторов. Разработаны пассивно-отказоустойчивые элементы и устройства, парирующие один, два и три отказа (сбоя) транзисторов. Выполнена оценка их эффективности, показывающая их предпочтительность перед мажоритарным резервированием. **Выводы**. Научная новизна полученных результатов заключается в следующем: проведены синтез и анализ пассивно-отказоустойчивых схем с «океаном» избыточности, обеспечивающем сохранение логической функции при заданном количестве отказов (от одного до трех). Затраты больше, чем на поддержание функциональной полноты в методе, ранее предложенном автором, но они того стоят. Несмотря на значительно большую избыточность по сравнению с мажоритарной избыточностью, энергопотребление оказалось ниже при незначительном увеличении задержки. Предложенные гиперотказоустойчивые ПЛИС целесообразно использовать в системах критического применения при невозможности технического обслуживания. В дальнейшем целесообразно рассмотреть вопрос резервирования на транзисторном уровне с использованием мостиковых цепей.

Ключевые слова: LUT; пассивно-отказоустойчивые системы; надёжность; избыточность.

ГІПЕРНАДЛИШКОВІСТЬ ДЛЯ НАДНАДІЙНИХ ПЛІС

С. Ф. Тюрін

Предметом дослідження, представленого в статті, є гіпернадлишкові елементи і пристрої ПЛІС, які можуть бути використані в високонадійних цифрових системах (ВНЦС). **Метою** даної роботи є розробка гіпернадлишкових логічних елементів, елементів пам'яті, буферних елементів для ВНЦС на основі ПЛІС, їх

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моделювання і оцінка надійності. **Задача**: розробити відмовостійкі логічні елементи LUT на одну, дві і три змінні. Розробити відмовостійку статичну оперативну пам'ять, Д-тригер і буферний елемент. Виконати симуляцію в NI Multisim для підтвердження працездатності та оцінки складності і споживаної потужності. Вивести формули для оцінки надійності розроблених елементів і пристроїв та побудувати графіки порівняння з відомими методами троірованія. Використовувані **методи**: введення надмірності на рівні транзисторів, методи моделювання в Multisim, математичні оцінки кількості транзисторів, розрахунки надійності. Були отримані наступні **результати**: при резервуванні логіки на транзисторному рівні і використанні послідовно-паралельних ланцюгів необхідно мінімум почетверення кількості транзисторів. Розроблено пасивно-відмовостійкі елементи і пристрої, що відображають один, два і три відмови (збою) транзисторів. Виконано оцінку їх ефективності, яка показує їх перевагу перед мажоритарним резервуванням. **Висновки**. Наукова новизна отриманих результатів полягає в наступному: проведено синтез і аналіз пасивно-відмовостійких схем з «океаном» надмірності, що забезпечує збереження логічної функції при заданій кількості відмов (від одного до трьох). Витрати більше, ніж на підтримку функціональної повноти в методі, раніше запропонованому автором, але вони того варті. Незважаючи на значно більшу надмірність в порівнянні з мажоритарною надмірністю, енергоспоживання виявилося нижче при незначному збільшенні затримки. Запропоновані гіпервідмовостійкі ПЛІС доцільно використовувати в системах критичного застосування прі неможливості технічного обслуговування. Надалі доцільно розглянути питання резервування на транзисторному рівні з використанням мостікових ланцюгів.

Ключові слова: LUT; пасивно-відмовостійкі системи; надійність; надмірність.

Тюрін Сергій Феофентовіч - Заслужений винахідник Російської Федерації, доктор технічних наук, професор кафедри автоматики і телемеханіки, електротехнічний факультет, Пермський державний технічний університет, Перм, Росія; професор кафедри математичного забезпечення обчислювальних систем Пермського державного національного дослідницького університету, механіко-математичний факультет, Пермь, Росія.

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