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ADAPTATION OF FPGA ARCHITECTURE FOR ACCELERATED IMAGE PREPROCESSING

The work is devoted to the topical problem at the intersection of communications theory, digital electronics and numerical analysis, namely the study of image processing methods implementation time on different architectures of computational devices, which are used for software and hardware acceleration. ***The subject*** *of this article is the investigation of reconfigurable FPGA processing systems in the image processing area.* ***The goal*** *of this work is to create a reconfigurable FPGA-based image processing system and compare it with existing processing architectures.* ***Task.*** *To fulfill the requirements of this work, it is necessary to prepare a practical experiment as well as theoretical research of the proposed architecture; to investigate the process of creating a ZYNQ SoC-based image processing system; and to develop and benchmark the speed of execution for the given set of algorithms with the specific range of the picture resolution.* ***Methods used:*** *FPGA simulation, C++ parallel programming with OpenMP, NVIDIA CUDA, performance analysis tools.* ***The result*** *of this work is the development of a resilient SoC Zynq7000–based computing system with programmable logic and the possibility to load images to FPGA RAM using the resources of ARM core for further processing and output via HDMI video interface, which enables the change of PL configuration at any time during the processing process.* ***Conclusions.*** *The efficiency of the FPGA approach was compared with a parallel image processing method implementation with OpenMP and CUDA. An overview of the ZYNQ platform with specific details related to media processing is presented. The analysis of algorithm speed testing findings based on various outputs proved the advantage (of over 60 times) of hardware acceleration of image processing over software analogs. The obtained results may be used in the development of embedded SoC-based solutions that require acceleration of big data processing. Also, the achieved findings can be used during the process of finding a suitable embedded platform for a certain image-processing task, where high data throughput is one of the most desired requirements.*

Keywords: *speedup; FPGA; performance; acceleration; parallel system; image processing.*

Introduction

The present-day development of various areas of human activity is tightly coupled with the development of information technologies, digital devices, and digital signal processing. IT development and digitization are intensively integrated in spheres that combine scientific research and engineering practice. Along with this, the mathematical tool, special-purpose technologies, input signal type (seismic vibrations, visible object images, acoustic vibrations etc.), software and hardware base as well as the demands put forward within problem definition vary depending on the application domain (radiolocation and radionavigation, oil production, space research, medical facilities, manufacturing, military hardware, science) of the digital signal processing theory [1].

Digital signal processing theory is tightly connected with disciplines such as data communication theory, numerical analysis, probability theory, statistical analysis, analog electronics, and digital electronics.

Having analyzed the abovementioned, it can be stated that the solution to the problem, which is at the intersection of various disciplines, is quite topical. An example of such task is the application of special-purpose computing devices for digital image processing algorithm acceleration.

Digital image processing is a form of information processing and conversion, in which data input is presented in the form of images (photos and video frames).

Image processing aims at producing a different image as an output or different attributes of the incoming image [2]. In addition, a necessity often emerges to process images that change in time, for instance, films and videos. The spheres of practical application of image processing methods are numerous: law, military science, medical establishments, aviation and space exploration, archives and electronic libraries, multiservice networks and the Internet [3, 4], weather services, law enforcement agencies etc.

Fig. 1 also displays digital image processing methods, which can be implemented on different software and hardware platforms. Depending on the need, processing may be done with the application of: CPU, which is enough for fulfilling the majority of everyday tasks [5]; GPU with SIMD-based architecture [6]; and FPGA,

which enables the avoidance of execution of extra instructions and gives the developer full control of the data flow [7].

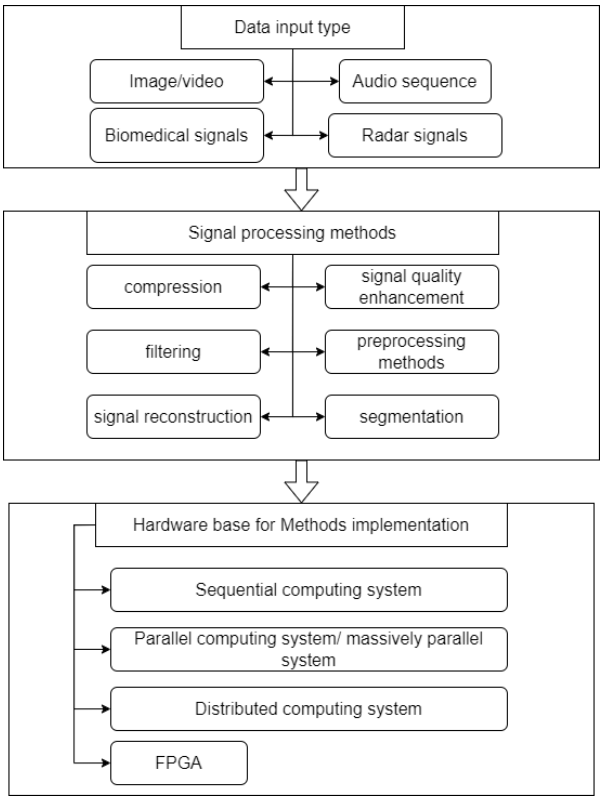

Fig. 1. Problem area analysis

One of the given boards is Xilinx Zynq 7020-based Z-turn Board (Fig. 2), which includes ARM Dual-core Cortex A9 (PS) and Kintex-7 (PL). PS may operate at a frequency of up to 866MHz and supports up to 1GHz DDR SDRAM. PL has 53200 LUTs, 106400 Flip-Flops, 140x36Kb RAM and 220 DSP blocks. The board itself fully caters for the minimum number of peripherals.

Overall, all the systems for prototyping SoC-based software and hardware solutions are similar by a series of factors. As a rule, systems on the chip combine the functional components of the whole device. They consume less energy, are less costly and work more efficiently than chipsets with the same functionality. Fewer components simplify the assembly of the finished product. One of the most popular SoC is Zynq7000 series by Xilinx (Fig. 3), which has two cores (ARM + FPGA) and provides a variety of interfaces for establishing communication (data exchange) between them.

Vendors of breadboards and software and hardware solutions debugging boards attempt to add as many peripherals as possible and provide maximum variability of their settings. The availability of HDMI, Ethernet, SD, USB HS and USB UART is the minimum for the given systems.

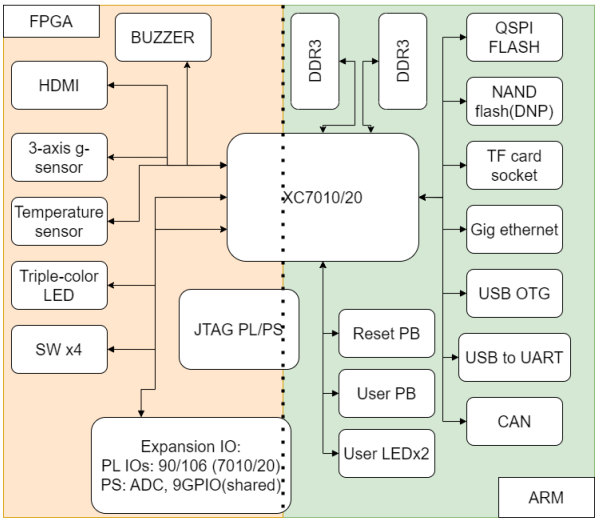

Fig. 2. Flow Diagram
for Z-turn Board Components [8]

Research task rationale. Related works

SoC-based system integration remains a practical area for both research and the platform development process.

Modern embedded systems contain complex firmware as well as the peripheral interconnections between the modules. The current requirements for most applications to be developed include:

– big output data processing capacity;

– original problem solution time improvement;

– usability and understandability features of the developed application;

– ease of scalability and modification;

– competitive development cost;

– etc.

Hardware computational power may help to meet the first two requirements from the abovementioned list. Due to the fact that Moore's law has been thrown overboard, yet the necessity to increase the computational capacity still exists, it is only possible to meet the requirements for computing and big output data processing speedup via the application of parallel processing as well as targeted computer devices adapted for special tasks execution [10, 11].

The works [12, 13] show that CPU and GPU-based computing systems can be used equally effectively to speedup image preprocessing methods. However, the obtained acceleration depends on the opportunity for algorithm' decomposition for the decomposition of the algorithm.

In [14, 15], attention is paid to the approaches to data parallelism organization and techniques of output data segmentation with the definition of computation granularity regarding the type of hardware base.

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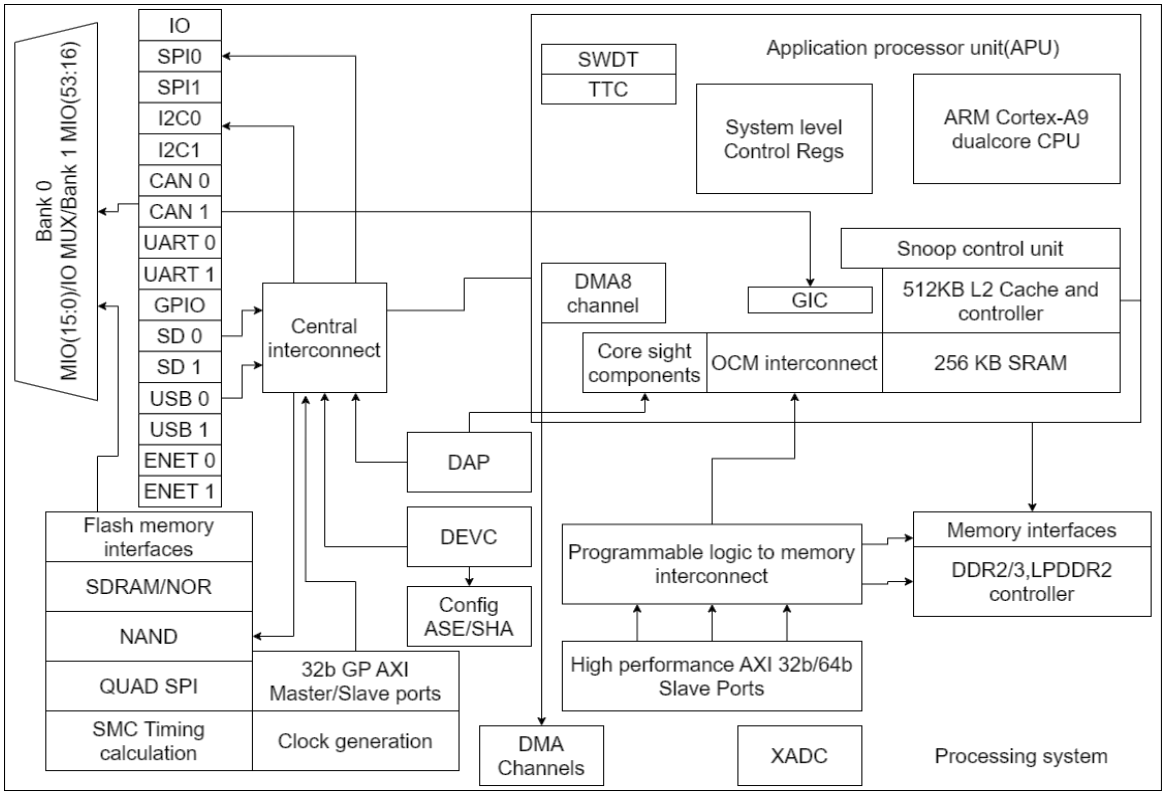

Fig. 3. Interface Flowchart for Xilinx Zynq7 [9]

Massively parallel architecture also justifies the need in GPU-based computations for general-purpose problem solutions [13, 16]. Application of CUDA technology along with the computing resource of a graphic processing unit (Nvidia Tesla K20) provides a speedup of up to 376 times during ultrasound image analysis and up to 426 times in problem solution aimed at aerial target identification based on infrared ray reflection time.

Modern FPGAs gain increased value in the application of software processors to solve several tasks, as mentioned in [17 – 19].

FPGA devices provide a series of sequential and parallel configuration interfaces [20] that can be used for loading configuration data. As a rule, the process of uploading bitstream requires the stop of chip operation; however, there are some devices that support dynamic partial reconfiguration (DPR).

FPGA-based systems use special-purpose equipment for logic processing. Unlike program solutions, which use context switching to maintain several threads, FPGA proposes real concurrent and special processing, in which tasks do not compete for access to the resources [21].

This support of multithreading must, in theory, provide for the reduction of time needed to perform naturally parallel tasks. The practical grounding for these theoretical findings is a task of high actuality and, thus, applied in practice.

All of the above gives reason to believe that the efficiency' and performance' research of a software and hardware computational complex based on FPGA [21] is an urgent task and can eliminate such problems in the field of image processing as:

– reducing of the image processing execution duration;

– computational device scalability;

– computational device portability.

Perspective studies related to special areas of image processing, such as machine vision for autonomous driving or medical image analysis, clearly shows the potential of using FPGA to accelerate processing in this domain area. In [20], attention is paid to the problem of implementation of the edge detection algorithm using Sobel operator. The corner cases of low data latency are mentioned as significant ones. Also, the implementation of Sobel algorithm is compared between general purpose CPU and Zynq-based FPGA platform. There is also the proposal of using reconfigurable facilities of the hybrid SoC, where the high-complexity image filtering was implemented via the hardware configuration [23].

The image defogging algorithms are covered in [24], where modern Vivado HLS tools are used for custom IP core generation. The aspects of HLS Synthesis for image processing are mentioned. Also, the output to a custom display with VDMA is implemented. The existing trends of using FPGA acceleration for cloud services allow us to implement the model of the top of multiple

FPGAs, which is known as FPGA-as-a-Service (FaaS). The topics related to the intercommunication delay between the nodes and reliability aspects are covered in [25]. Meanwhile, the aspects of embedded system reliability remain actual through the history of programmable logic. There are existing tools for simulation and failure detection of FPGA designs during the development process, but the practical aspects may differ from the theoretical ones. The experience in operating and analytical reliability assessment of FPGA is covered in depth in work [26], where the practical aspects are also mentioned in the summary.

Aim and tasks of the work

The aim of this study is to design a resilient Zynq7000 SoC-based hardware accelerator for further research into the processing speed of a programmable logic computing device exemplified by image preprocessing tasks.

The designed software and hardware complex should be resilient in further exploitation and development. In the case of the proposed system, resilience can be defined like the ability to continue and process the given information under adverse conditions or stress, even if debilitated state is reached.

Achieving the set aims requires the following tasks to be solved:

– study the interaction of SoC system components;

– design a Zynq7000 SoC-based hardware accelerator;

– design FPGA-based system architecture in the real-time;

– implement SoC-based image processing algorithms in Verilog on a single-processor computer and in a massively parallel system with high processing quality preservation;

– conduct the analysis of research findings.

Therefore, concerning the capacity of the selected system, it is possible to set certain requirements for hardware accelerator features, including:

– program interfaces for the interaction of a processing subsystem (PS) and programmable logic (PL);

– ability to upload images in PL RAM;

– display of the processed image via HDMI video interface;

– real-time PL configuration updatability.

Materials and methods

The following image processing tasks were selected for the experiments: noise suppression, image transformation into the grayscale, binarization of the grayscale image, and morphological transformation [1]. A selection criterion is the natural parallelism of most studied methods and their frequent use.

Testing is performed on computing devices with varying architectures, namely:

– single-processor computing system;

– massively parallel computing system;

– field-programmable gate array.

The research of the performance of the single-processor computing system was conducted on the basis of developed software using the C ++ language and the OpenCV library (version 4.2.0). The graphical user interface was built on QtWidgets. A computer with AMD A6-7310 2.4 GHz processor (RAM 8 GB 2600 MHz) was used to test the performance of the selected digital image processing algorithms on the CPU in sequential mode.

To measure the serial algorithm time execution, the capabilities of a standard library were used. The determination of the execution duration is shown in program listing 1.

```
int
DeviceCPU::MeasureExecution(std::function<
void()> func) {
    using namespace std::chrono;
    using timestamp =
time_point<high_resolution_clock>;
    timestamp t_before =
high_resolution_clock::now();
    func(); // execute algorithm
    timestamp t_after =
high_resolution_clock::now();
    return duration_cast<milliseconds>(t_after
- t_before);
}
```

Listing 1. Sequential CPU timing

The research of the performance of the massively-parallel computing system was conducted on the basis of developed software using the CUDA technology (CUDA Toolkit 10.0 for the minimal compute capability 3.0 and the driver version 411.31) and OpenCV library with additional set for C and C ++ development.

To measure the parallel algorithm time execution, the capabilities of CUDA-events were used. The execution time determination is shown in program listing 1 and 2.

To design a FPGA-based image processing system, the “B-PDPR: Follow-behavior” pattern was used, and the “A-PDPR: Data-exchange” architectural pattern was used for interaction between program tasks.

The architectural part presents four tasks, replacing each other, depending on the current state. The data stream is formed sequentially for each item. Once the data have been processed, they are transferred to the next task (Fig. 4 and 5).

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```
int
DeviceGPU::MeasureExecution(std::function
<void()> cuda_f){
    float elapsed=0;
    cudaEvent_t start, stop;
    HANDLE_ERROR(cudaEventCreate(&start));
    HANDLE_ERROR(cudaEventCreate(&stop));
    HANDLE_ERROR(cudaEventRecord(start,
nullptr));
    cuda_f(); // execute
    HANDLE_ERROR(cudaEventRecord(stop,
nullptr));
    HANDLE_ERROR(cudaEventSynchronize (stop));
    HANDLE_ERROR(cudaEventElapsedTime(&elapsed,
start, stop));
    HANDLE_ERROR(cudaEventDestroy(start));
    HANDLE_ERROR(cudaEventDestroy(stop));
    return static_cast<int>(elapsed);
}
```

Listing 2. Parallel GPU timing

The engineered architecture for real-time FPGA image processing allows you to perform the necessary calculations without worrying about the current state of the program and reconfiguration. The system can be easily expanded to more algorithms if needed.

Design of the programmable gate array computing device

In compliance with these requirements, the designed device has program interfaces necessary for the interaction of the microprocessor control unit with programmable logic, which facilitates uploading images to PL memory. In addition, the processed image output via HDMI video interface and real-time PL configuration is available.

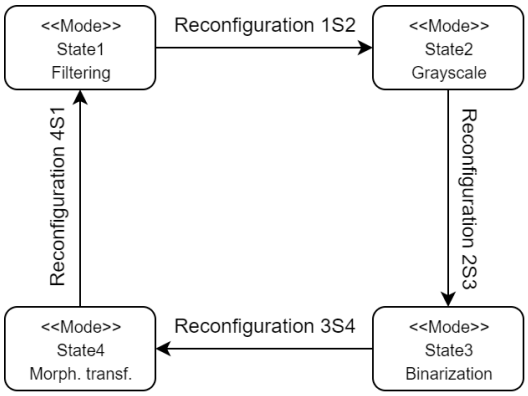

Fig. 4. "B-PDPR: Follow-behavior" template state change diagram

The dataflow chart inside the SoC system is shown in Fig.6. The following IP blocks by Xilinx were used in the design (Fig. 7):

– ZYNQ7 Processing System is responsible for PL+PS integration and peripherals configuration;

– Block Memory Generator provides an interface for accessing BRAM;

– AXI BRAM Controller and AXI SmartConnect enable PS interaction with BRAM via AXI bus line.

Processor System Reset and Clocking Wizard – generate clocking and asynchronous reset signals.

Within the implementation of the median filter, a scheme allowing input of two vectors, which represent pixel component values concerning the color of a digital image and communicate them to the outputs depending on their size, was developed for comparing every matrix element (Fig. 8).

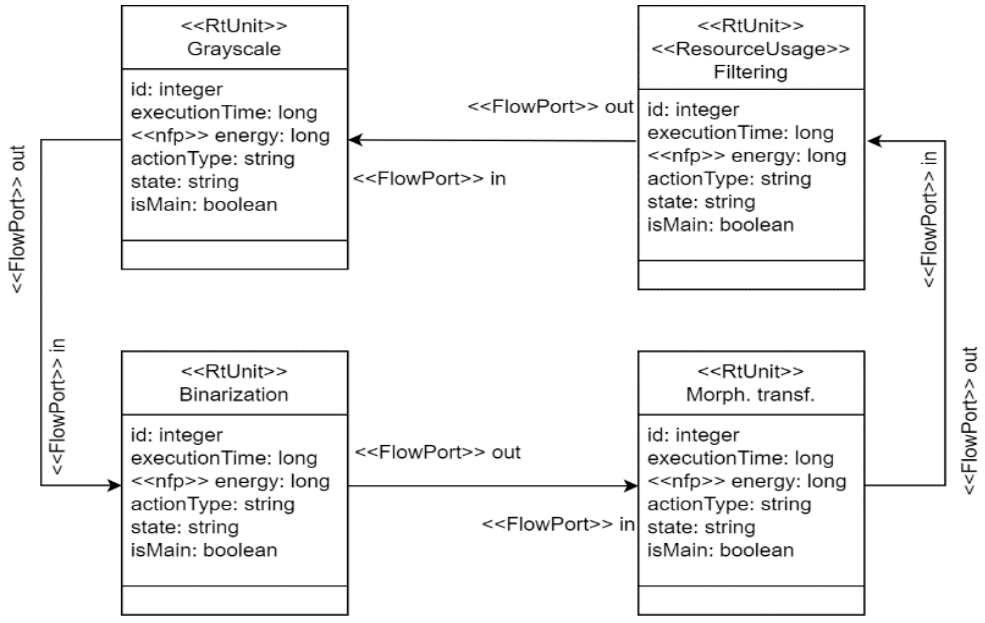

Fig. 5. "A-PDPR: Data-exchange" template state change diagram

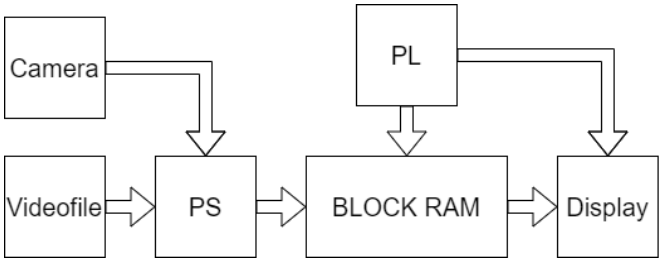

Fig. 6. Design Dataflow Chart

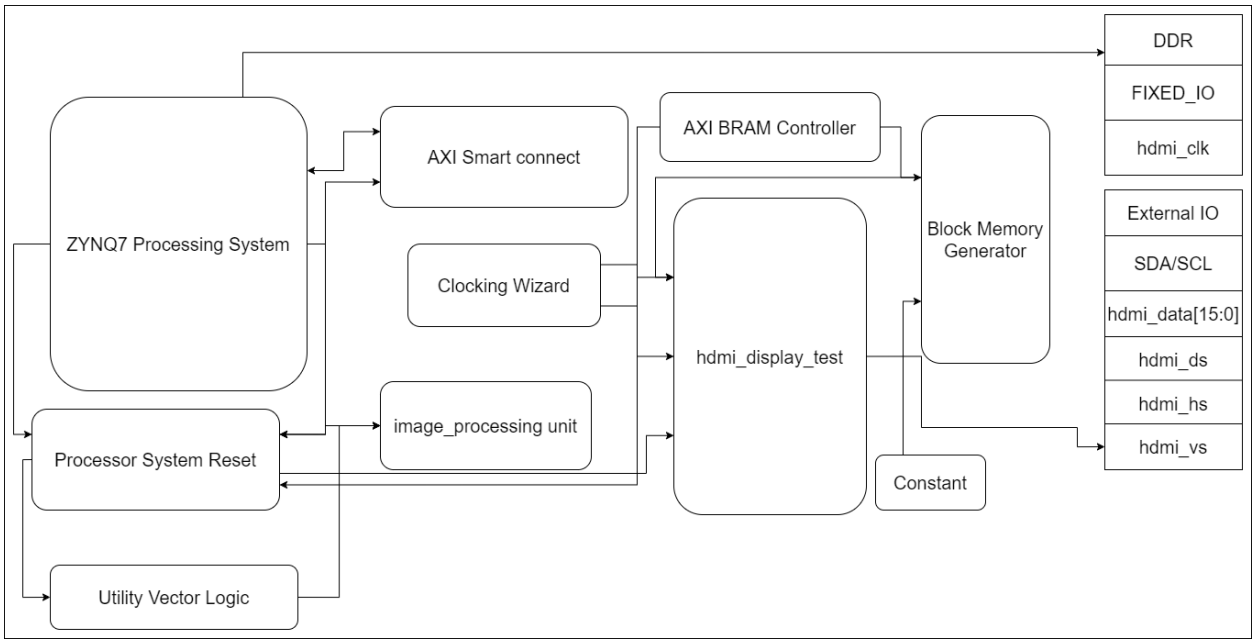

Fig. 7. General Design Structure Chart

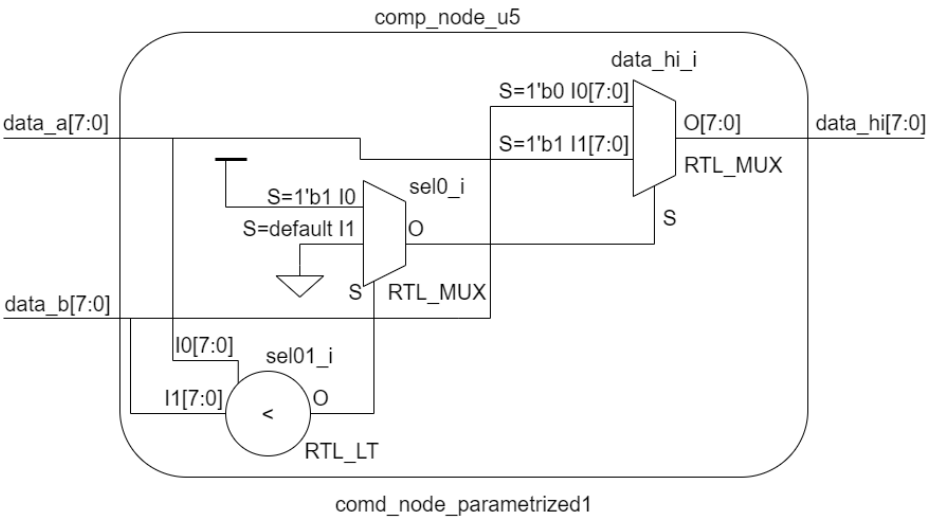

Fig. 8. RTL Scheme for Designed Element

The median filter is used in digital image and signal processing in the process of digital filtering for noise suppression. Input data are a two-dimensional matrix, the samples from which are arranged in ascending or descending order, and the value within the ordered list enters the filter output.

Nine plus one elements of this kind are needed for calculating the median value for a 3x3-sized matrix (Fig. 9).

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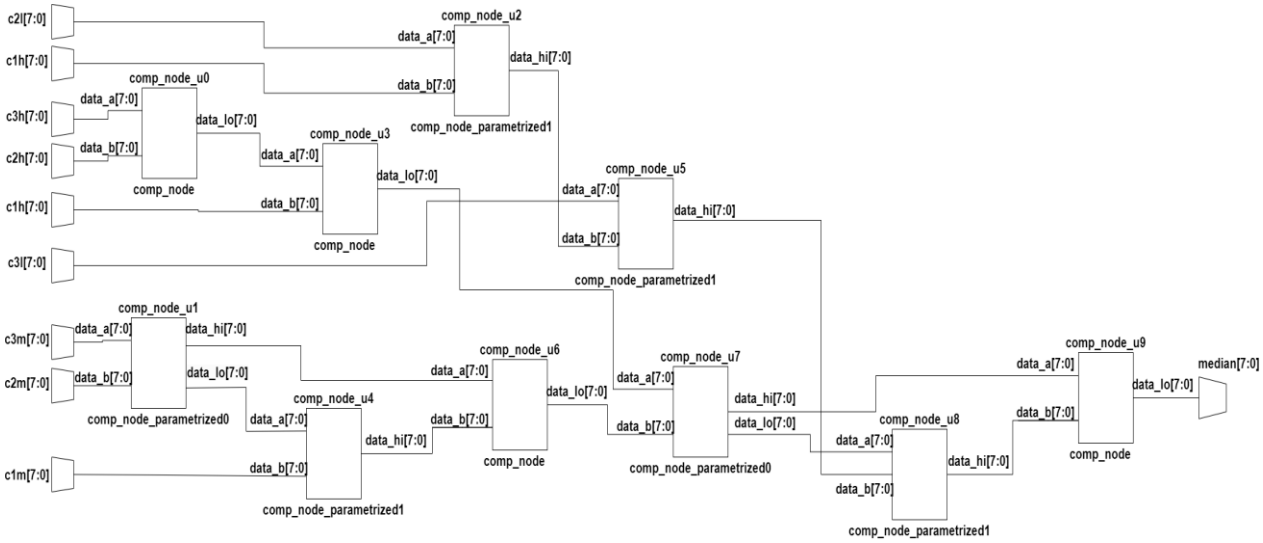


Fig. 9. RTL Scheme of Device for Median Value Calculation

Noise suppression from the color image requires the definition of the median value with the account taken of every color channel (RGB). Therefore, the whole algorithm does not require additional work cycles and is executed via a combinational circuit. The end device is shown in Fig. 10. The simulation findings prove that processing of one image pixel in the filter takes one clock signal pulse (Fig. 11).

To transform a color image into a grayscale image, finding the arithmetic mean of the channels for every pixel is enough.

After the vector division operation, the total amount of clocking signal cycles necessary for obtaining the result equals 2 (see Fig. 11).

To transform a grayscale image into a binary image, the thresholding algorithm is applied. Its main idea lies in one or several threshold values. If the input numeric color value exceeds the threshold value, the output color is white, if it does not, the output color is black (see Fig. 11, b).

Development of image output

Xilinx Zynq7020-based Z-turn Board has SiI9022A video transmitter controlled with PL (Fig. 12). The transmitter receives RGB888 (24bit) formatted data, but the board design restricts the use of data lines and is set for the work with RGB565 (16bit) format.

Interaction with the transmitter requires the use of two clock domain signals (see Fig. 12 and Fig. 13). Data and the address are generated separately and I2C protocol is used for operation with VDMA.

ARM core in Zynq7020 system is operated by OS Linux. Block RAM of SoC memory is accessed via a special device file, thus, data can be sent and received using a memory-mapped file region.

OpenCV library was used to simplify digital image processing in PS. The result of software to be used in PS retrieves each image from the video file (or a camera) frame by frame and transmits it to PL for further processing and display on the screen. The main indicator of the developed device quality assessment is the data processing speed compared with the program solutions.

The findings made after the application of the abovementioned methods are provided in Fig. 14.

Experiment, Results and Discussions

Research was conducted on the basis of the developed software with the use of C++ and OpenCV library (version 4.2.0).

A computer with the following configuration in order to test the speed of the selected digital image processing algorithms on the CPU: AMD A6-7310 2.4 GHz processor (8 GB 2600 MHz RAM, OC Windows 10 Home x64).

Median filter was selected as the algorithm for color image filtering with the time slot and search box size is 3x3 pixels.

Thresholding algorithm was applied to convert the filtered color image into a grayscale image and further into a binary image with the starting brightness value of 50.

Morphological transformations included opening and closing operations with 10x10 pixel cores. The obtained results for color images with various resolutions

after progressive processing by every algorithm are presented in Table 1. The table contains the execution time for the selected algorithms with the different input image size. The measurement unit is milliseconds. The table row contains the image input size and 4 algorithms runtime duration on CPU.

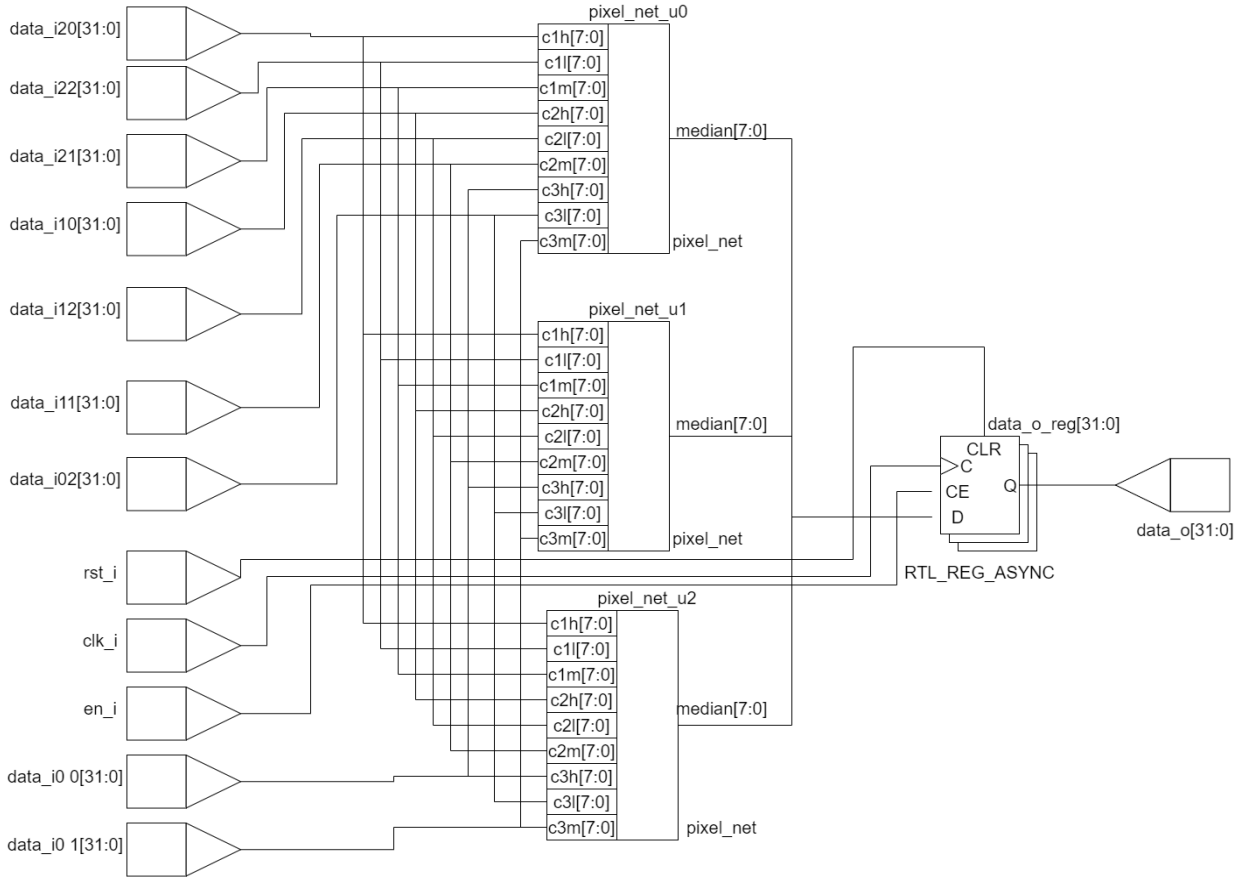
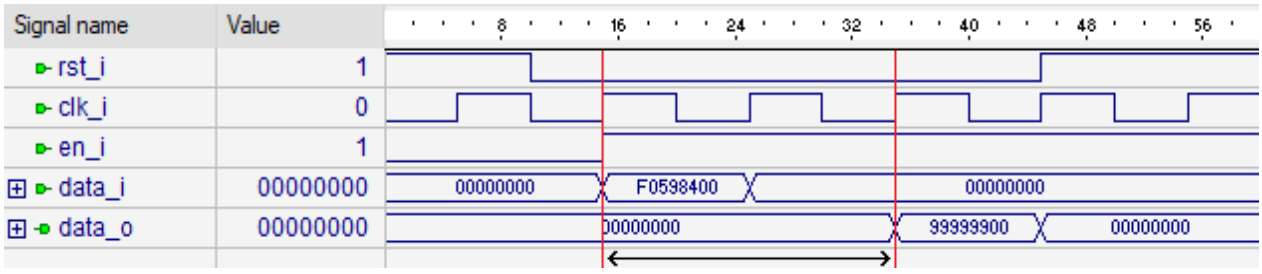
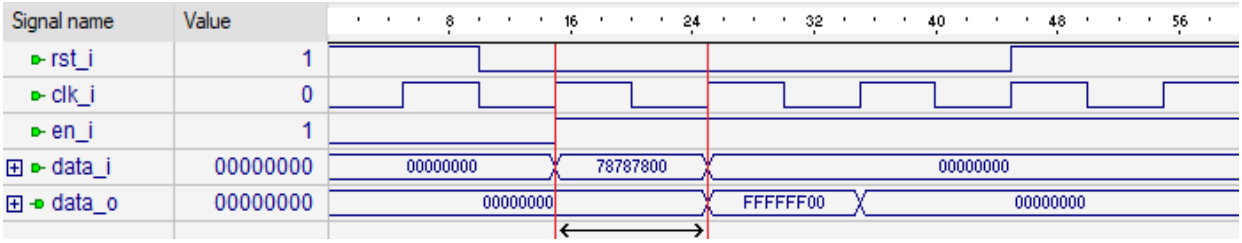


Fig. 10. RTL Scheme for 3x3 Median Filter



a)



b)

Fig. 11. Software-Based Simulation Findings:
a) for converting to grayscale image, b) for converting to binary image

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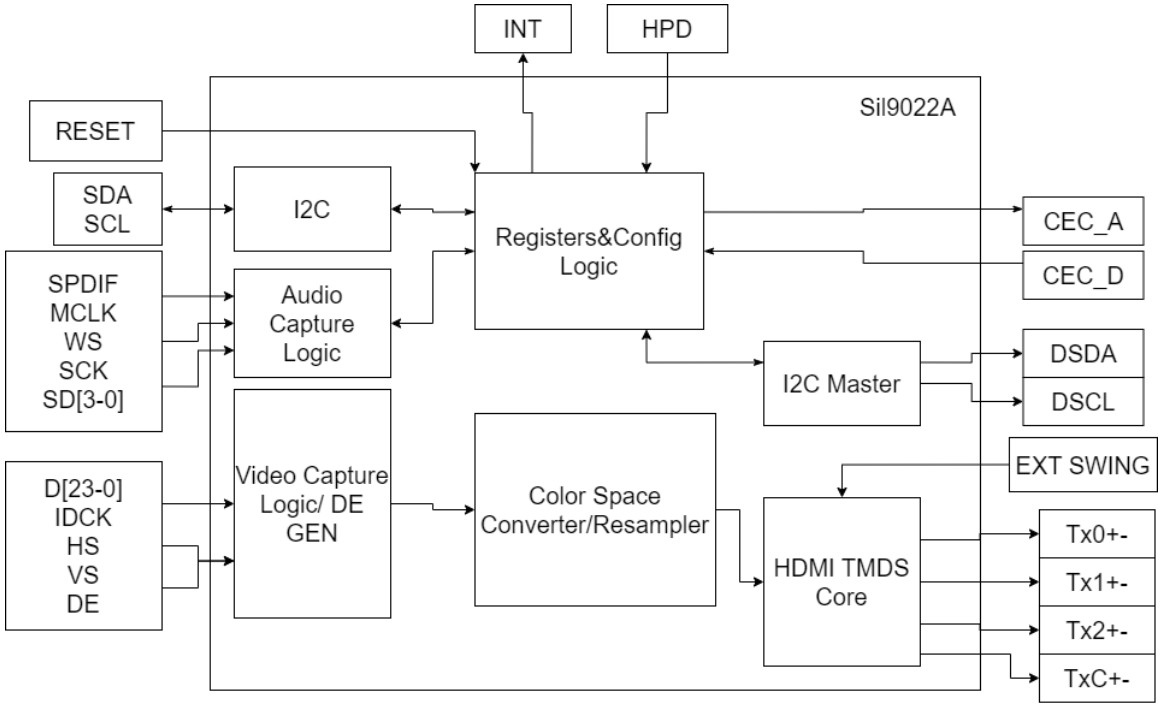
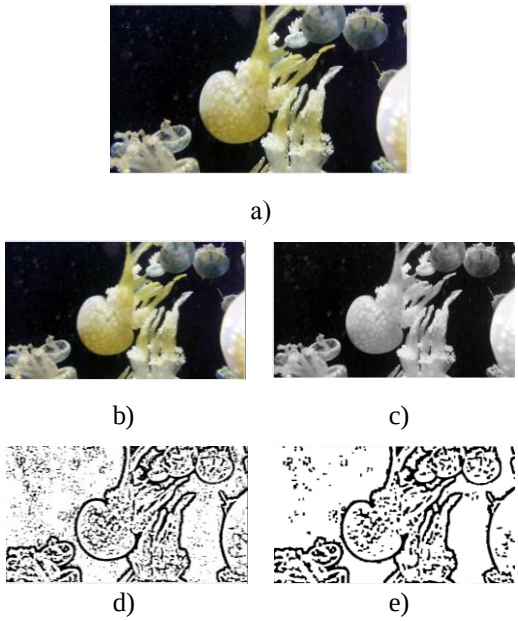


Fig. 12. Core Transmitter Structure Chart

Output Clock	Port Name	Output Freq (MHz)	
		Requested	Actual
clk_out1	clk_out1	100.000	100.000
clk_out2	clk_out2	148.500	148.438

Fig. 13. Clocking Signals Settings



a)

b) c)

d) e)

Fig. 14. Results of application of the tested digital image preprocessing methods: a) output image; b) the result of noise suppression; c) grayscale image; d) binary image; e) the result of morphological transformation

Table 1

Results of image processing algorithms on CPU

Input image size	Algorithm time (ms)			
	Image filter	Grayscale	Binarization	Morph transf.
1920x1080	723	110	23	850
1280x720	322	42	10	380
640x480	163	18	4	130
320x240	84	10	1	34

NVIDIA CUDA, which provides for the full range of applications for development in C and C++ was To ensure simplicity, an OpenCV library enhancement, which encompasses various extensions on CUDA (CUDA Toolkit 10.0), was applied.

All algorithms applied in program implementation on GPU fully comply with the analogs on CPU. All input data and parameters come in the same way and have equal values. Output data are provided in Fig. 14.

Testing was conducted on NVIDIA Quadro K2000M GPU. The device has 384 CUDA cores and 2 GB DDR3 global memory with 128-bit bus width. The shared memory size is 48Kb, the clock rate is 750 MHz.

Data allocation for the algorithms was done in global memory. The time slot for data allocation and copying into GPU was neglected in the end values. The time of the regarded methods' implementation is shown in Table 2. The table structure is similar to Table 1, but the results are shown for the same algorithms, but executed on GPU.

Table 2

Results of image processing algorithms on GPU

Input image size	Algorithm time (ms)			
	Image filter	Grayscale	Binarization	Morph transf.
1920x1080	86	3	1	23
1280x720	45	2	1	14
640x480	22	1	1	9
320x240	14	1	1	8

Obtained Results

To estimate the image processing module execution speed, start_i and done_o signals were used. Therefore, having calculated the number of clocking signal pulses between these two events, it was possible to obtain the time necessary for full processing of one image. The comparison results are presented in Table 3 and Figures 15-17.

Table 3

Execution Time Comparison Chart

1920x1080	Execution time (ms)		
	CPU	GPU	FPGA
Image filter	723	86	12
Grayscale	110	3	4
Binarization	23	1	2

As metrics for the analysis of the results obtained, we used the practical speedup of the studied image processing methods on the designed and developed software and hardware complex based on FPGAs with respect to sequential implementation on the CPU and parallel implementation on the GPU. The speedup was calculated in accordance with:

$$S_{FPGA(base)} = \frac{T_{base}}{T_{FPGA}},$$

where T_{base} is the task execution time on the CPU or GPU, T_{FPGA} is the task execution time on the developed FPGA-based computing system.

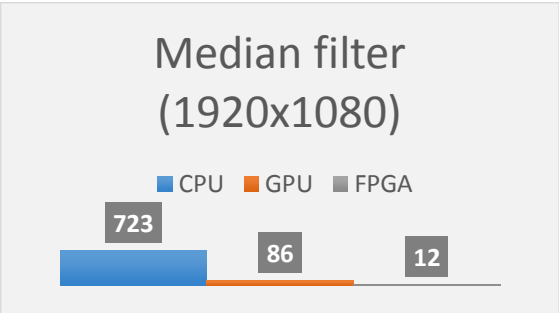


Fig. 15. Filtering Algorithm Running Speed Comparison

The implementation of the existing sequential image filtering algorithm based on the median filter takes a significant amount of time ($T_{CPU} = 723$ ms), as shown on the blue bar of the chart (Figure 15). The specialized graphics processor provides an execution time $T_{GPU} = 86$ ms. Thus, the highest obtained speedup of the developed software and hardware computing complex based on FPGA leads to $S_{FPGA(CPU)} = 60.25$ relative to the sequential execution time on the CPU.

The implementation of sequential converting an image to grayscale takes a significant amount of time ($T_{CPU} = 110$ ms), as shown on the blue bar of the chart (Figure 16).

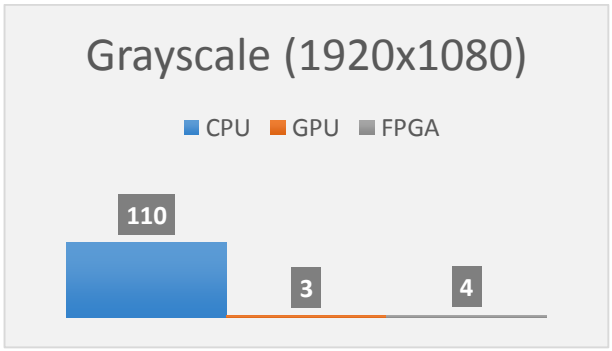


Fig. 16. Color Conversion Algorithm Running Speed Comparison

The specialized graphics processor provides an execution time $T_{GPU} = 3$ ms. The developed software and hardware computing complex based on FPGA provides an execution time $T_{FPGA} = 4$ ms and does not give the highest speedup for color conversion algorithm running. This is due to the architectural features of the NVidia company graphics processors.

The situation is similar to binarization algorithm running (Fig.17). The time of the binarization algorithm execution on the GPU and on the developed computer complex differs by 1ms and show an acceleration of almost 20 times.

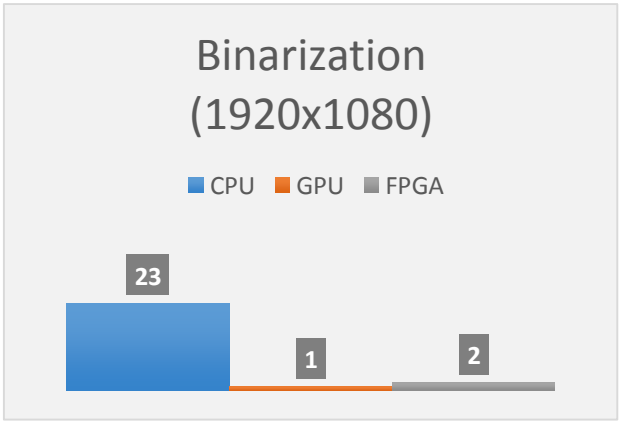


Fig.17. Binarization Algorithm Running Speed Comparison

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A comparative analysis was conducted for the results of algorithm running speed testing on various input data, which demonstrated the significant advantage of hardware acceleration of image processing over their software analogs.

Conclusions

The result of the work is the research conducted into the capabilities of a SoC Zynq7000-based hardware accelerator on the example of image preprocessing compared with massively parallel systems and parallel shared memory computing systems.

The advantage of the designed software and hardware complex with programmable logic is the ability to load images to FPGA RAM using the resource of ARM core for further processing and display via HDMI video interface, in which PL configuration can be changed at any time within the processing process, and this makes the system resilient in further exploitation and development. For the designed software and hardware, complex resilience can be defined as the ability to continue and process the given information under adverse conditions or stress, even if a debilitated state is reached. The results of the execution are well defined among the system launches, and essential operation capabilities are maintained. The system is extensible by using partial reconfiguration facilities, which add an extra isolation layer from the architectural and development perspective.

A comparative analysis was conducted for the results of algorithm running speed testing on various input data, which demonstrates the considerable superiority (by over 60 times) of hardware image processing acceleration over their software analogs.

In conclusion, it should be noted that the advantage of the developed software and hardware computing complex based on FPGAs is that it is easily expandable and reconfigurable for most image processing methods. However, just for the problem of filtering based on the median filter, the proposed and developed system gives a high acceleration, reaching up 60 times. This confirms the need for hybrid computing to achieve maximum efficiency in computer graphics problem execution.

The obtained results can be applied in the development of embedded SoC-based solutions that require big data processing acceleration.

Thus, the work shows that the solution of the problem posed on the basis of FPGA is an alternative to special-purpose integrated circuits and can reduce image processing time execution. This is important in many fields of science and technology where the time of filtering, transformation and binarization of the image stream is critical (for example, processing information from satellites when compiling maps of the area, identifying objects in computer vision systems, analyzing the kinematics of human body movement in medical systems, and so on). Compared to other hard-coded logic solutions, FPGAs have the advantage of being flexible and programmable in nature. Also, most modern FPGA devices support dynamic partial reconfiguration, which enables the possibility of performance increasing in comparison to computing on a conventional computer.

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АДАПТАЦІЯ FPGA АРХІТЕКТУРИ ДЛЯ ПРИСКОРЕННЯ АЛГОРИТМІВ ОБРОБКИ ЗОБРАЖЕНЬ

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Ця робота присвячена актуальній проблемі на перетині теорії зв'язку, цифрової електроніки та чисельного аналізу, а саме вимірюванню часу виконання методів обробки зображень на різних архітектурах обчислювальних пристроїв, які забезпечують програмне та апаратне прискорення. **Предметом** вивчення статті є дослідження реконфігурованих FPGA систем в області обробки зображень. **Метою** цієї роботи є створення перероблювальної системи обробки зображень на базі FPGA та порівняння її з існуючими архітектурами обробки. **Завдання:** Для виконання вимог роботи необхідно підготувати практичний експеримент, а також теоретичне дослідження запропонованої архітектури; дослідити процес створення системи обробки зображень на основі ZYNQ SoC; розробити та порівняти швидкість виконання для заданого набору алгоритмів із певним діапазоном роздільної здатності зображень. **Використані методи:** симуляція FPGA, паралельне програмування на C++, технологія NVIDIA CUDA, інструментарій для аналізу продуктивності виконання програм. **Результатом** цієї роботи є розробка стійкої обчислювальної системи на базі SoC Zynq7000 з програмованою логікою та можливістю завантаження зображень в RAM FPGA з використанням ресурсів ядра ARM для подальшої обробки та виводу через інтерфейс відео HDMI, що дозволяє змінювати конфігурацію PL у будь-який момент під час обробки. **Висновки.** Ефективність підходу FPGA порівнювали з реалізацією методів паралельної обробки зображень за допомогою OpenMP та CUDA. Представлено огляд платформи ZYNQ з конкретними деталями, пов’язаними з обробкою медіа. Аналіз результатів тестування швидкості алгоритму на основі різних виходів довів перевагу (у понад 60 разів) апаратного прискорення обробки зображень перед програмними аналогами. Отримані результати можуть бути використані при розробці вбудованих рішень на базі SoC, які вимагають прискорення обробки великих даних. Крім того, отримані результати можна використовувати під час пошуку відповідної вбудованої платформи для певного завдання обробки зображень, де висока пропускна здатність системи є однією з найбільш пріоритетних вимог.

Ключові слова: прискорення обробки даних; FPGA; висока продуктивність; паралельні системи; обробка зображень.

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