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INFLUENCE OF THE NUMBER SYSTEM IN RESIDUAL CLASSES ON THE FAULT TOLERANCE OF THE COMPUTER SYSTEM

*The concept of increasing the fault tolerance of a computer system (CS) by using the existing natural redundancy, which depends on the number of systems used, is considered. The **subject** of this article is the methods and means of increasing the fault tolerance of CS and components based on the use of a non-positional number system in residual classes. It is shown that the use of the system of residual classes (SRC) as a number system ensures the fault-tolerant functioning of the real-time CS. This study considers a fault-tolerant CS operating in the SRC. The **aim** of this research is to show the influence of the non-positional number system in the SRC on the possibility of organizing the fault-tolerant functioning of a computer system. The **object** of this research is the process of fault-tolerant functioning of the CS in the SRC. This article provides an example of the operation of a fault-tolerant CS in the SRC given by a set of specific bases. The fault tolerance of CS in the SRC is ensured by the use of the basic qualities of the SRC by the method of active fault tolerance by using the procedure of gradual degradation. The level of fault tolerance of CS in the SRC in the example given in the article is achieved by reducing the accuracy of the calculations. This article considers two levels of degradation. Variants of algorithms for operating fault-tolerant CS in the SRC in the modes of replacement and gradual degradation are presented. Methods of system analysis, number theory, theory of computing processes and systems, and coding theory in the SRC were the basis of the conducted research. The **results** of the analysis of the specific example of the functioning of CS in the SRC given in the article, specified by four information and one control bases, showed the effectiveness of using non-positional code structures to ensure fault-tolerant operation. **Conclusions.** This article discusses the concept of increasing fault tolerance based on the use of the existing primary redundancy contained in the CS, due to the use of the basic properties of the non-positional number system in residual classes.*

Keywords: computational tract; fault tolerance; fault-tolerant computer system; number system; primary redundancy; reservation methods; system of residual classes.

Introduction

A further possible promising way of improving computer systems (CS) is to increase the main parameters (speed, productivity and reliability) of their functioning. Therefore, recently the question of researching new or improving existing methods of improving the fault tolerance of the CS is widely discussed and relevant [1].

Motivation

The need to increase the requirements for ensuring the high speed of integer arithmetic operations and the reliability of CS and components of CS (CCS) determines the constant search, research, development and implementation of new, promising information technologies and data processing methods, oriented, in particular, to the area of integer arithmetic calculations [2].

The theory and global practice of creating high-performance CSs have shown that it is fundamentally impossible to achieve a significant increase in speed

within the limits of binary positional number system (PNS) [3]. At the same time, long-term theoretical research and results of practical implementation, conducted toward the development of the theory and practice of non-positional coding of data in the system of residual classes (SRC) and its use for the construction of high-performance CSs, have shown the high efficiency of the use of non-positional coding. In addition, the results of the analysis of modern trends in the development of CS and CCS functioning in the SRC confirm the presence of the following conflict situation in non-positional computer machine arithmetic. On the one hand, there is a contradiction between the existing possibilities of significantly increasing the speed of performing integer arithmetic operations in the SRC [4]. On the other hand, the insufficient level of fault tolerance of functioning cannot ensure high reliability of the CCS operating in the SRC, which reduces the overall reliability of the CS. At present, the currently existing models and methods of increasing the fault tolerance of the CCS operating in the SRC do not sufficiently consider the influence of the basic qualities of the SRC on the structure and princi-

ples of the operation of the CS [5]. This circumstance necessitates the formulation and solution of a new, important, and relevant scientific and technical problem – the development of models and methods for increasing the fault tolerance of CS and CCS operating in the SRC, without reducing the implementation speed of integer arithmetic operations.

State of the Art

Modern research literature is replete with information about various aspects of fault tolerance of the CS, described methods and means of improving fault tolerance in CS, which are gradually losing their effectiveness. However, the application of non-positional number systems, which based on the Chinese remainder theorem, as an effective tool for increasing the reliability characteristics, including the fault tolerance of the CS, is an insufficiently researched area.

D. K. Pradhan [6] carried out the full-fledged study in this area was at the end of the 20th century. The author provides an exhaustive discussion on designing computer systems that are resistant to different types of faults, emphasizing hardware and software redundancy mechanisms [6]. Despite providing comprehensive coverage, the book does not consider alternative numbering systems such as the SRC.

P. Castaldi et al. analyzed and discussed an active fault-tolerant control system that relied on a nonlinear geometric approach for fault diagnosis, which ensured fault tolerance of the system [7]. Yet, the work does not cover the use of the SRC as a strategy for achieving fault tolerance.

Ch. Hajiyeu and H. E. Soken [8] provide a comprehensive examination of fault tolerance and system reliability, with detailed discussions of fault-tolerant fault filtering algorithms. However, they did not consider the SRC in their discussion, which could be used in these algorithms.

A detailed review of the literature shows that the application of the SRC, as a number system of CS, to improve fault tolerance has not adequately investigated. While significant work has been done in the broader field of fault tolerance, the specific potential of SRC remains underexplored. This article aims to fill this gap by presenting novel concepts, classifications, and a case study that demonstrate the potential of the SRC to enhance the fault tolerance of the CS. At present, there is a growing research interest in the application of SRC for fault tolerance, as evidenced by the following recent publications:

- Selianinau examined the effectiveness of the non-positional number system and proposed a minimally redundant residue number system (RNS, another name for the SRC) [9]. Based on this, a new method was pro-

posed to provide low computational complexity and high fault tolerance of the rank calculation [10];

- in [11], the authors proposed a novel approach to construct a RNS using redundant residue representations. This redundant RNS construction is designed to enhance error detection and correction, thus improving fault tolerance. However, this approach results in higher costs for performing addition and multiplication operations. While the authors acknowledge the need for further investigation to improve the efficiency of their proposed RNS, the study does not explore the inherent properties of non-positional number systems such as RNS for enhancing fault tolerance in a broader context;

- in [12], the authors introduce readers to various ways of designing computational systems depending on the use of non-traditional counting systems, such as Residue Number System, Logarithmic Number System, Redundant Binary Number System and others. Analysis of the impact of the considered calculation systems showed that the use of non-positional RNS, due to the use of basic properties, has a positive effect on the improvement of the main characteristics of the CS, including fault tolerance.

Common in these works is the focus on the process of data processing in the non-positional number system, the use of the properties of non-positional data coding in SRC, which ensures fault-tolerant operation of the CS.

In addition, a detailed literature review analyzed key works on fault tolerance, which take into account the different types of redundancy, and active fault tolerance. For example, the works of Professor V. S. Kharchenko propose new original scientific directions in the field of creating reliable and fault-tolerant real-time computer systems operating in the PNS [13-15].

Objectives and novelty

This article presents an in-depth study of an innovative **approach** to increasing the fault tolerance of CS, in particular, using a non-positional number system in residual classes. This article clarifies some definitions and presents a classification of various ways to achieve CS fault tolerance within the SRC framework. The result of this classification directly or indirectly determines the selection, justification, and application of the necessary methods for increasing fault tolerance, depending on the field of application of computing structures.

The **object** of this research is the process of fault-tolerant functioning of the CS in the SRC.

The **aim** of this study is to show the influence of the non-positional number system in the SRC on the possibility of organizing fault-tolerant functioning of a computer system.

The novelty and relevance of the research conducted in this article are as follows. The **novelty** of this research is that for the first time the influence of SRC on the fault tolerance of the CS is considered. The **relevance** of this research is due to the following circumstances. First, there is a need to maintain an operational state of real-time CS. Second, the results of recent studies have shown that the use of a non-positional number system as a number system in residual classes has improved some characteristics of the CS. However, the lack of research into the influence of SRCS on the fault tolerance of computing structures hinders the practical implementation of non-positional code structures.

1. Fault tolerance and reliability of the CS

The fault tolerance of the CS is the property of the CS to function without fail in the event of one or more failures in the hardware and software of the CS. It is possible to use another definition of the concept of fault tolerance of the CS. The fault tolerance of the CS is a property of its architecture as a digital and logical data processing system, which provides it with the ability to function without fail in accordance with the given problem-solving program [16].

Suppose that at the design stage, it is necessary to ensure a given level of reliability of the system. It is possible to increase (ensure) reliability if the system has a certain property, the use of which will allow it to be done. Such a property is defined as fault tolerance [17]. Regarding the CS, the concept of failure tolerance can be understood as the property of the CS that ensures its operational state in the event of failure of the elements included in their composition. In defining the term fault tolerance, three main aspects of its use are distinguished:

- the property of fault tolerance is established by the developers when designing the CS to increase its reliability;
- the required level of fault tolerance is achieved mainly when using redundant (additional) technical means (introduction of artificial structural and (or) other redundancy) compared to the minimum required to perform all the necessary functions of the CS in full;
- the use of the fault-tolerance property allows for maintaining full or partial operability of the CS.

Ensuring (increasing) fault tolerance of the CS requires the presence of various types of redundancy. First, the presence of redundant hardware and software of the CS is required. There are two main practical methods of increasing fault tolerance for the CS operating in the PNS. The first method for increasing fault tolerance is to increase the fault-freeness of the CS elemental base. The second method of increasing fault tolerance is the introduction of various types of redundan-

cy [18] in the CS (application of various methods and types of reservation).

According to the method of implementation, active and passive fault tolerance are distinguished. Active fault tolerance of the CS is based on the procedure for performing the following main sequence of operations:

- operational data control;
- diagnostics of failures;
- error correction;
- reconfiguration of the CS structure.

From the above, it is obvious that the organization of the procedure of active fault tolerance of the CS involves the development and application of methods of operational data control, diagnosis, and correction of errors. With passive fault tolerance, the failure of the CS may not manifest itself at all (for example, CS in the PNS with a majority reserve). There is a mixed active-passive fault tolerance. Moreover, in CS, passive fault tolerance is carried out at the level of the element base, and active fault tolerance is usually carried out at the level of multi-processor CS.

The relationship between the known concept of system reliability and system fault tolerance can be defined as follows. System fault tolerance is a means of maintaining system reliability [19]. Fault tolerance supports the reliability of CS. The fault tolerance of positional CSs is ensured by introducing additional redundancy, as a rule, by introducing structural redundancy into the CS. At the same time, the possibility of using redundancy, which is contained at the expense of the number system (NS), is not considered in the positional CS.

With the traditional approach to the NS, which is used in modern CS, the following basic requirements are put forward:

- ease of technical implementation of the representation of code words when using the existing element base;
- the unity of the presentation of code words in a given numerical range;
- ease of hardware and software implementation of methods and algorithms for performing necessary operations (primarily arithmetic operations) in a given NS;
- fulfilment of the "economical" condition of the NS, which characterizes the primary redundancy of the CS [12].

In [20], regarding data processing tools, notions of primary and secondary redundancy of CS were introduced. In general, these concepts can be generalized and described as follows:

Definition 1. The primary (structural, informational, functional) redundancy (PR) of CS is called existing or artificially introduced redundancy of this type because of the nature of the creation or the method of artificial formation of the used NS.

Definition 2. The secondary (structural, informational, functional, temporary, and load-bearing) redundancy (SR) of the CS is the redundancy artificially introduced into the CS to improve its individual characteristics (performance, reliability, fault tolerance, interference immunity, etc.) after the NS is finally determined.

It can be seen from the second definition that SR is a redundancy caused by the use of traditional reservation methods, which are widely used in technical systems for various purposes to improve their characteristics. PR for CS coincides with the concept of natural redundancy (NR) of technical data processing systems, and SR coincides with the concept of artificial redundancy (AR).

2. Influence of the number system on the fault tolerance of the CS

When researching and developing methods for increasing the reliability of the CS, it is expedient and convenient to divide the concept of fault tolerance into two components, i.e. use two separate terms: natural and artificial fault tolerance [6]. The introduced terms are convenient to use when analyzing and synthesizing the reliability structures of CS. These concepts quite fully reflect the essence of calculation methods for increasing the reliability of CS. Let us define these terms.

Definition 3. The natural fault tolerance (NFT) of CS is the property of CS to maintain a functional state due to the use of NR only.

Definition 4. Artificial fault tolerance (AFT) of CS is a property laid down in the design of CS, the use of which allows maintaining a functional state in case of element failures due to the simultaneous use of NR and AR.

Obviously, NFT determines the inherent (existing) level of system reliability, while AFT determines the aggregate (required, set) level of reliability. The general task of reliability enhancement can be expressed as ensuring the fault tolerance of the CS through the simultaneous use of NR and AR. The enhancement of reliability, as a feature of system dependability, can be achieved through either passive or active fault tolerance methods.

Definition 5. The method of passive fault tolerance is a method of increasing fault tolerance through concurrent utilization of NR and AR without reconfiguring (constant reservation) of the CS structure. This method is used during the design phase to elevate the system reliability to a pre-specified (required) level of fault tolerance.

Definition 6. The method of active fault tolerance is a method of increasing fault tolerance through concurrent utilization of NR and AR by reconfiguring (dynamic reservation) of the CS structure. This method is

also employed during the design phase to augment the system reliability to a pre-specified (required) level of fault tolerance.

The need to introduce and use SR is determined by the requirements for the characteristics of the created CS. Along with the above-mentioned requirements for the NS, note that the selected and used NS itself significantly affects the following characteristics of the CS:

- the structure (architecture) of the CS;
- principles of information processing;
- the requirements for the use of the new element base of the CS;
- speed of implementation of arithmetic operations;
- system and user productivity (performance) of the CS;
- reliability, survivability, accuracy and fault tolerance of the CS;
- operational characteristics and indicators of the CS, etc.

Quantitatively, the volume of CS equipment V_{PR} determined by the presence of PR is slightly less than the amount of equipment V_{NR} in the presence of NR.

The volume of additional equipment of the CS V_{SR} determined by the presence of SR, completely coincides with the volume of equipment V_{AR} determined by the presence of the AR. The analysis of the influence of NS on the structure and individual characteristics of different types of CS showed that for digital information processing systems it is correct to assume that $V_{PR} \approx V_{NR}$.

The following condition is ensured by the existing procedure for determining the NS of CS:

$$V_{PR} = \min. \quad (1)$$

It is obvious that the fulfillment of condition (1) is not always appropriate when the a priori problem of improving the reliability of CS characteristics arises due to the introduction of various types of redundancy. It is quite possible that the variant of creation of the CS, based on the fulfillment of condition (1), is not expedient. This feature manifests itself when using SRC as a CS number system. Consider this assumption.

3. Fault tolerance of the CS operating in the SRC

It is known that the excessive CS in the SRC contains a larger (by $\approx 15-20\%$) amount of equipment V_{PR} than CS in the binary PNS. In the last one, the data is provided and is processed by a positional binary code, given the same length of the bit grid of CS and with the same requirements presented to CS without considering

the introduction of SR [12]. However, as shown by theoretical studies and practical calculations [5], to achieve the pre-specified (required) level of fault tolerance $F(t)$

of the CS in the SRC, a much smaller amount of equipment is required than for the CS in the PNS (Table 1).

Table 1
Estimated data on the relative number of conditional equipment of CS in PNS and CS in SRC

l (n)	PNS (binary)		SRC				Winning ratio δ
	$V_{PR}^{(1)}$	$V_{\Sigma}^{(1)}$	Information bases	Control bases	$V_{PR}^{(1)}$	$V_{\Sigma}^{(1)}$	
1 (4)	8	24	$m_1=3, m_2=4, m_3=5, m_4=7$	$m_5=11, m_6=13, m_7=17$	10	23	4
2 (6)	16	48	$m_1=2, m_2=5, m_3=7, m_4=9, m_5=11, m_6=13, m_7=17, m_8=19$	$m_9=23, m_{10}=29, m_{11}=31$	19	34	29
3 (8)	24	72	$m_1=3, m_2=4, m_3=5, m_4=7, m_5=11, m_6=13, m_7=17, m_8=19, m_9=23, m_{10}=29, m_{11}=31, m_{12}=37, m_{13}=41$	$m_{14}=43, m_{15}=47, m_{16}=53$	28	43	40
4 (10)	32	96	$m_1=2, m_2=3, m_3=5, m_4=7, m_5=11, m_6=13, m_7=17, m_8=19, m_9=23, m_{10}=29, m_{11}=31, m_{12}=37, m_{13}=41, m_{14}=43, m_{15}=41, m_{16}=53$	$m_{17}=59, m_{18}=61, m_{19}=67$	37	54	43
8 (17)	64	192	$m_1=2, m_2=3, m_3=5, m_4=7, m_5=11, m_6=13, m_7=17, m_8=19, m_9=23, m_{10}=29, m_{11}=31, m_{12}=37, m_{13}=41, m_{14}=43, m_{15}=47, m_{16}=51$	$m_{17}=53, m_{18}=57, m_{19}=59$	67	82	57

Preliminary calculations showed that the total structural redundancy of CS in SRC $V_{\Sigma} = V_{PR} + V_{SR}$, that provides a given level of fault tolerance $F(t)$ much less than that for duplicated and tripled majority computing structures widely used in the PNS, i.e., the condition is satisfied:

$$\begin{cases} F_{SRC}(t) \geq F_{PNS}(t) [t = \text{const}]; \\ V_{\Sigma_SRC} < V_{\Sigma_PNS}. \end{cases} \quad (2)$$

Condition (2) is valid without reducing the speed of performing arithmetic operations of CS.

Expression (3) determines the opposite condition to condition (2), i.e. with the same (equal) amount of equipment V_{Σ} in the SRC provides a higher value of fault tolerance $F(t)$, i.e.:

$$\begin{cases} F_{SRC}(t) > F_{PNS}(t) [t = \text{const}]; \\ V_{\Sigma_SRC} \approx V_{\Sigma_PNS}. \end{cases} \quad (3)$$

Table 1 presents the estimated data on the relative number of conventional CS equipment (computing structures) reduced to one binary digit of the 1-byte bit grid of the CS in PNS and SRC. The necessary amount (number) of equipment is calculated according to the proposed method, where:

$V_{PR}^{(1)}$ – the relative number of conditional equipment of non-excessive CS in PNS and CS in SRC, given to one binary discharge of the 1-byte bit grid of CS;

$V_{\Sigma}^{(1)}$ – the relative number of conditional equipment of excessive CS in PNS (triple majority structure) and CS in SRC (with three control bases), given to one binary discharge of the 1-byte bit grid of CS;

δ – winning ratio of the amount of total equipment of CS in PNS and CS in SRC, where:

$$\delta = \frac{V_{\Sigma_PNS}^{(1)} - V_{\Sigma_SRC}^{(1)}}{V_{\Sigma_PNS}^{(1)}} \cdot 100\%.$$

The results of the calculations (Table 1) showed that with an increase in the length of the 1-byte bit grid of the CS, which is characteristic of the modern trend in the development of computing tools for processing digital information, the efficiency of the use of SRC increases significantly.

Let us consider the influence of the basic qualities of the SRC on the possibility of organizing the fault tolerance of the real-time CS. There are three basic qualities of SRC:

1. Independence of the functioning of the computational tracts of data processing of the CS in the SRC.

This property of SRC implies the possibility of synthesizing the structure of CS, which is similar to the structure of the reserved system in PNS. This circumstance makes it possible to create a CS structure in the form of a set of independent and parallel working computational tracts (CTs) of data processing [9]. In this case, the CS in the SRC has a modular design, which allows maintenance and elimination of CT failures by simply replacing an inoperable CT with a workable CT, without interrupting the solution of the task. Based on the structure of the CS, errors arising due to failures in one arbitrary CT always remain within the limits of this one CT. The use of this property makes it possible to create a system of continuous control, diagnosis and correction of errors, without stopping the solution of the task, which is important for CS operating in the real-time mode of data processing.

2. *Equality of the functioning of the computational tracts of data processing as part of the CS in the SRC.* The principles of the formation of numbers in the SRC show that any one residue of the number in the SRC carries information about the entire original number [10], which makes it possible to replace the CT modulo m_i that failed with any workable tract modulo m_j using known methods, provided that $m_i < m_j$ without interrupting the solution of the task. In the presence of failures in the third or fourth CT, the CS can continue to execute the calculation program with a certain decrease in the accuracy of the calculations; that is, the CS in the SRC has the property of gradual degradation. This property determines a characteristic feature of the functioning of the CS in the SRC: the computer system, depending on the requirements placed on it, can have different reliability, accuracy of calculations and speed of operation in real time. In this aspect, the following can be noted. In the process of implementation of the calculation task, if necessary, it is possible to change the indicators of reliability, accuracy and speed of operation of the CS. The use of the first and second properties of the SRC determines the simultaneous presence of three types of reservation in the CS: structural, informational and functional. Based on the idea of structural reservation, the joint use of the first and second properties makes it possible to synthesize mathematical models of the reliability of CS in the SRC, similar to models of permanent or dynamic reservation in PNS.

3. *A small bit grid of the computational tracts of data processing of the CS in the SRC.* This property makes it possible to increase significantly the fault tolerance, reliability, and speed of the CS. This is achieved both because of the low-bitness of construction of the CTs CS in the SRC and because of the possibility of using (unlike PNS) tabular arithmetic [21], where the basic arithmetic operations are performed practically in

one machine cycle of CS operation. In particular, the low-bitness of the residues in the representation of the SRC numbers makes it possible to choose various options for circuit-technical solutions when implementing modular arithmetic operations based on the following principles:

- the adder principle (based on the use of low-bit binary adders by modulo);
- the tabular principle (based on the use of small-sized Read-Only Memory (ROM) units);
- the ring shift principle (based on the use of ring shift registers).

Due to the influence of the basic qualities of the SRC (independence, equality and low-bitness residues, $a_i \equiv A(\text{mod } m_i)$, $i = \overline{1, n}$, representing a number) on the peculiarities of CS synthesis, structural, informational and functional reservation have a simultaneous and mutually positive effect on each other. For example, the introduction of secondary structural redundancy (application of structural reservation) with the help of additional use of k reserve CTs to the available n main ones, leads to the manifestation of both informational and functional reservation. Information reservation is associated with information redundancy due to the presence of redundant code words and implemented by using additional information obtained from the outputs of k reserve CTs [22]. Regarding functional reservation, according to the properties of the SRC, one operable CT CS in the SRC, functioning by bases of m_j , if the condition is met:

$$m_j \geq \prod_{p=1}^r m_{ip}, \quad (4)$$

can take over the computational functions of up to r simultaneously CTs that have failed.

The manifestation of the basic qualities of the SRC explains the content of mathematical expressions (2) and (3) as follows:

- the primary redundancy present in the CS operating in the SRC manifests itself noticeably and significantly positively (from the point of view of improving the reliability of the CS) only in the presence of secondary redundancy;
- in the CS in the SRC there is a significant mutual positive influence at the same time of individual types of reservation provided for increasing the fault tolerance $F(t)$ of the CS.

In contrast to SRC, in the PNS the use of one type of reservation does not always lead to the simultaneous presence of other types of reservation, which is a sign of the absence of other types of reservation [8]. Thus, the use of information reservation (introduction of infor-

mation redundancy) to increase the reliability of CS calculations in the PNS causes the presence of structural SR. Thus, the application of the required type of reservation in the PNS is necessarily accompanied by the presence of a structural ("harmful") redundancy that is not used, which, in the end, negatively affects the technical and cost characteristics of the CS [23].

4. The structure of the fault-tolerant CS in the SRC

Let us consider the structure of a fault-tolerant CS using the example of a specific SRC. In Fig. 1 presents a block diagram of the fault-tolerant CS in the SRC, set

by the information bases $m_1 = 3, m_2 = 4, m_3 = 5, m_4 = 7$ and one control base $m_k = m_{n+1} = m_5 = 23$ SRC. Let us consider an example of a concrete implementation of the process of functioning of the fault-tolerant CS in the SRC (Fig. 1). Assume that the fault-tolerant CS has two levels of degradation ($j = 1, 2$) with the corresponding accepted values of $D_1 = 139$ and $D_2 = 61$.

For this SRC $D_0 = \prod_{i=1}^4 m_i = 420$, that is, the in-

formation range in which calculations are performed without degradation ($j=0$), is equal to $[0, D_0)$.

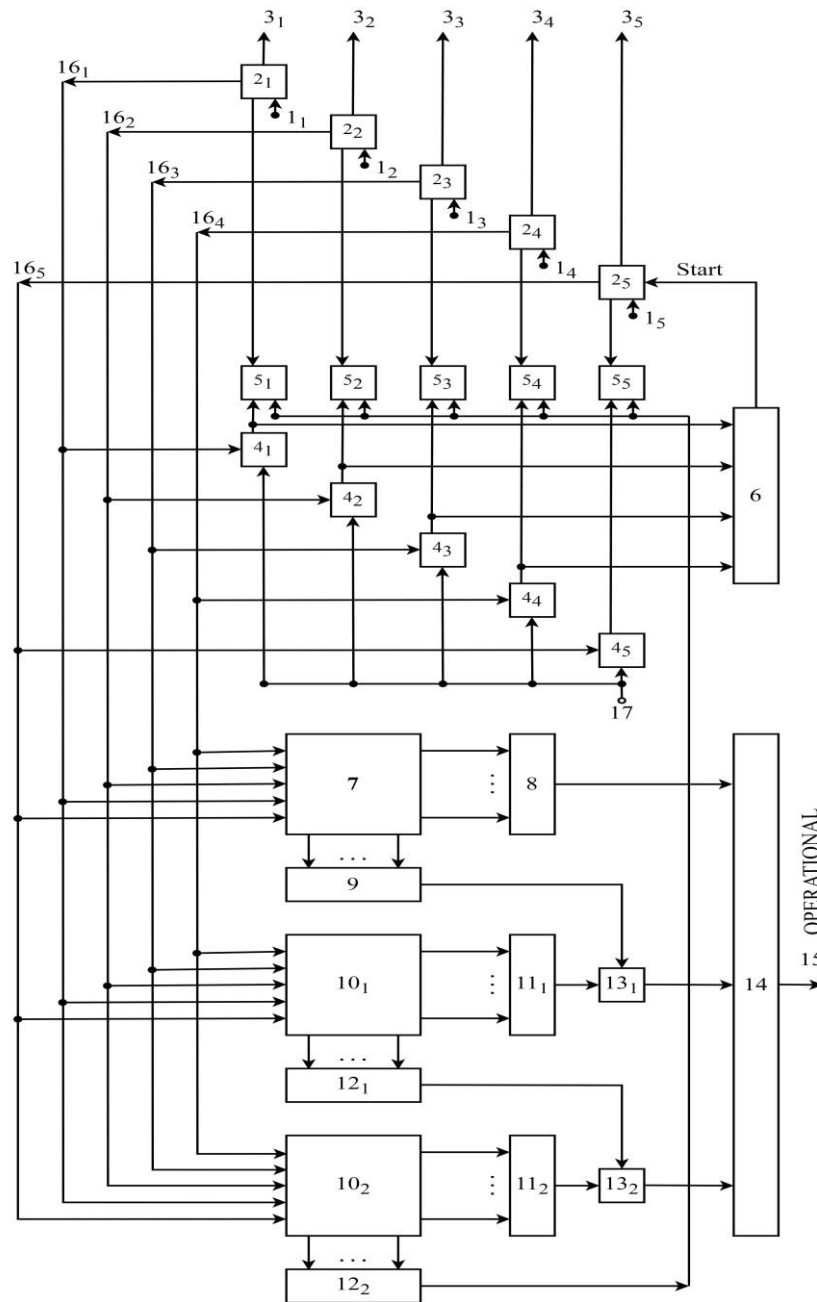


Fig. 1. Fault-tolerant CS in the SRC [24]

For the first ($j=1$) degradation level, this range is $[0, 139]$, and for the second ($j=2$) degradation level, this range is $[0, 61]$. The degradation conditions of each level (condition (4)) are defined as follows: for the first

degradation level $\prod_{z=1}^{Q_1} m_{i_z} \geq D_1$, for the second degrada-

tion level $\prod_{z=1}^{Q_2} m_{i_z} \geq D_2$. In general, the value of Q is the number of the SRC bases.

For the information range of calculations (zero level of degradation, $j=0$), the following relation determines the condition of normal functioning of the fault-

tolerant CS: $m_k = m_{n+1} = 23 \geq \prod_{p=1}^r m_{i_p}$, where r is the

number of operational CTs of the fault-tolerant CS.

The peculiarity of the functioning of the CS in the SRC lies in, in some cases (in the CT replacement mode), the possibility of replacing not one, but at the same time, several inoperable working tracts with a single operational control tract when condition (4) is met. This makes it possible to increase significantly the fault tolerance of the CS in the SRC due to the possibility of simultaneous use of three types of reservation. Structural reservation, due to the introduction of one control CT on the bases, which functions in parallel with the main (informational) CT. Information reservation due to the use of additional output information of the control CT, which provides the possibility of correcting distorted information. Functional reservation, due to fulfillment of condition (4).

In the article, the example given below shows that SRC, in contrast to PNS, introduced SR is used maximally to improve the characteristics of CS. Indeed, the use of any type of reservation ultimately leads to structural (hardware) redundancy [23], which in SRC (unlike PNS) is used to organize several different types of reservation at the same time, which increases the coefficient of use of redundant and general of total CS equipment introduced.

The article proposes a new concept of increasing the fault tolerance of CS. This concept is based on the use of the PR available in the CS, which is determined by the selected number system. Based on the above, when creating (designing) a CS, it is necessary to consider not only the influence of the NS on the volume of equipment V_{PR} , but firstly to estimate the value of V_Σ considering the influence of the NS on other characteristics of the CS. That is, it is advisable to choose the NS taking into account its further influence on the choice of methods improvement of the necessary characteristics of the CS. Apparently, when building highly fault-tolerant computing structures; it is possible to abandon

the traditional criterion of "economical" selection of positional NSs according to criterion (1).

As research and calculations have shown [12], it is advisable to choose the NS, from the point of view of ensuring a given level of fault tolerance of the CS, according to the criterion:

$$V_\Sigma = \min, \quad (5)$$

and not according to criterion (1), at a given level of requirements for individual characteristics of the CS. This problem is close to the task of optimal reservation in the theory of reliability, which was confirmed during the practical creation of blocks and nodes of fault-tolerant CS in SRC.

In the general form of a fault-tolerant CS in the SRC (see Fig. 1) with n information CTs and one control CT contains the following elements: $1_1 \div 1_{n+1}$ – the first (informational) inputs of the CS; $2_1 \div 2_n$ – information CTs; 2_{n+1} control CT; $3_1 \div 3_{n+1}$ – informational outputs of CTs; $4_1 \div 4_{n+1}$ – the first group of elements AND; $5_1 \div 5_{n+1}$ – the first group of elements OR; 6 – the first element OR; 7 – decoder (a device for converting a binary number code into a unitary number code); 8 – second element OR; 9 – third element OR; $10_1 \div 10_k$ – a group of decoders; $11_1 \div 11_k$ – the second group of OR elements; $12_1 \div 12_k$ – the third group of elements OR; $13_1 \div 13_k$ – the second group of elements AND; 14 – fourth element OR; 15 – output " OPERATIONAL " CS in the SRC; $16_1 \div 16_{n+1}$ – outputs of CS control blocks (units) in the SRC; 17 – clock input of the device. CS in the SRC can work in two modes. Let us consider each operating mode of the CS for an arbitrary the SRC with n informational CTs and one ($k=1$) control CT [24].

The first mode is a mode without degradation of the quality of the fault-tolerant CS functioning, i.e. without reducing the accuracy of calculations (data processing is carried out in the information range $[0, D_0]$). This is done under the following conditions: all information $2_1 \div 2_n$ and control 2_{n+1} CTs are operational; all information $2_1 \div 2_n$ CTs are operational, and control 2_{n+1} CT has failed; control 2_{n+1} CT is operational, and part of r information CTs from n total number of $2_1 \div 2_n$ CTs have failed; while condition (4) is fulfilled.

At the same time, the calculations will be carried out in the working information range $[0, D_0]$, where

$$D_0 = \prod_{i=1}^n m_i. \text{ The number of output buses } 16_1 \div 16_{n+1} \text{ of}$$

the CT control blocks $2_1 \div 2_{n+1}$ of the fault-tolerant CS equals the value of $n+1$. The presence of a signal on the i -th originating bus (a unit in the binary code of the CT control block states $2_1 \div 2_{n+1}$) CT control block 16_i condi-

tions the failure of the 2_i -th CT. The decoder 7 converts the original binary code of CT control block states into a unary code [19]. The first group of decoder outputs $10_1 \div 10_k$, which combine buses for which the original binary code of CT states defines the operational state of the fault-tolerant CS, are connected through OR elements 8 and 14 to the "OPERATIONAL" output 15 of the CS in the SRC.

The control signal for the mode without degradation is generated at the output of OR element 8. The signal or signals of the failure of the 2-th CT (or a set of the $2_1 \div 2_{n+1}$ CTs) also arrive at the first inputs of the AND elements $4_1 \div 4_{n+1}$, to the second inputs of which the clock bus signal 17 arrives. Through the open AND element 4_i (or AND elements $4_1 \div 4_n$), the signal (or signals) through the OR element 6 activates ("Start") the control CT 2_{n+1} by the base m_{n+1} , and simultaneously, the original signal (or signals) of the AND element (AND elements $4_1 \div 4_{n+1}$) through the corresponding OR element (or elements) $5_1 \div 5_{n+1}$ disables the corresponding CT (or CTs) $2_1 \div 2_{n+1}$. If there is a set of inoperative informational CTs $2_1 \div 2_{n+1}$ and condition (4) is not met, then the fault-tolerant CS is considered to have failed.

The second mode is a mode with degradation of the quality of the fault-tolerant CS functioning, that is, with a decrease in the accuracy of calculations. The control signal for the first ($j=1$) level of degradation is formed at the output of the OR element 9. The control signal for the $(i+1)$ -th level of degradation is formed at the output of the OR element 12_k . Let us assume the j -th level of degradation is implemented. In this case, the original signal from the $(j-1)$ -th OR element 12 serves as a control signal for the CS in the degradation mode. In this case, when the condition is met:

$$\prod_{z=1}^{Q_j} m_{i_z} \geq D_j, \quad (6)$$

where Q_j – the number of the SRC bases; calculations will be carried out in a numerical range $[0, D_j)$. If condition (6) is met, then the signal from the decoder output 10_j through the OR element 11_j , the open AND element 13_j , and the OR element 14 is sent to the "OPERATIONAL" output 15 of the CS. Simultaneously, the signal (or signals) from the output buses $16_1 \div 16_{n+1}$ of the control blocks, corresponding to the CTs $2_1 \div 2_{n+1}$ of the CS through the corresponding open AND elements 4 and corresponding OR elements 5 disable the corresponding CTs among the possible CTs $2_1 \div 2_{n+1}$. If condition (6) is not met, then the signal from the second group of decoder outputs 10_j through the OR element 12_j opens the $(i+1)$ -th AND element 11_{k+1} .

In other words, this signal serves as a control signal for the $(i+1)$ -th level of degradation.

Table 2 shows the operating conditions of the fault-tolerant CS in the SRC. Where the value Ω_j ($j=0,1,2$) is the number of elements of the set of operational states of the CTs (a sign of the operational capability of the fault-tolerant CS is the arithmetic sign "+" in columns 3, 5 and 6 of Table 2), respectively, to the operating modes Ω_j ($j=0,1,2$) of the fault-tolerant CS. For the first operating mode of the fault-tolerant CS ($j=0$) (without degradation) the number of operational states of the CTs $\Omega_0=10$ is equal to the number of output buses of the first group of outputs of the decoder 7 (that is, the number of "+" signs in column 3 of Table 2). For the second operating mode of the fault-tolerant CS ($j=1$) (the first level of degradation) the number of operational states of the CTs $\Omega_1=14$ is equal to the number of output buses of the first group of outputs of the decoder 10_1 (that is, the number of "+" signs in column 5 of Table 2). For the second operating mode of the fault-tolerant CS ($j=2$) (the second level of degradation), the number of operational states of the CTs $\Omega_2=19$ is equal to the number of output buses of the first output group of the decoder 10_2 (that is, the number of "+" signs in column 6 of Table 2).

The second group of outputs of decoders 7, 10_1 and 10_2 , which unify buses with numbers corresponding to the inoperable states of the CTs of the fault-tolerant CS (arithmetic sign "-" in columns 4, 6 and 8 of Table 2), are connected according to the inputs of the OR elements 9, 12_1 and 12_2 .

5. Modes of operation of the fault-tolerant CS in the SRC

Let us consider the first (without degradation) mode of functioning of the fault-tolerant CS.

Variation 1.1. All CTs $2_1 \div 2_5$ are operational. In this case, from the outputs of the CT control block $2_1 \div 2_{n+1}$ via buses $16_1 \div 16_5$ the binary code of the CTs states (of the form 00000) is sent to the input of decoder 7. The signal from the zeroth output is then passed through the OR element 8 and OR element 14 to the "OPERATIONAL" output 15 (see Table 2, columns 1-4).

Variation 1.2. All CTs $2_1 \div 2_4$ are operational, whereas the control CT 2_5 is inoperable. The binary code representing the states of CTs, 10000, is transmitted via buses $16_1 \div 16_5$ to the input of decoder 7. The signal from its output goes through the sixteenth output bus, then via OR elements 8 and 14 to the "OPERATIONAL" output 15 (see Table 2, columns 1-4).

Table 2

Operating conditions of the fault-tolerant CS in the SRC

Indicators of outputs buses 16 ₁ ÷16 ₅ of control blocks					Numbers of CTs of the fault-tolerant CS which have failed	The first mode		The second mode			
m ₅	m ₁	m ₂	m ₃	m ₄		Correlation of information m ₁ + m ₄ and control m ₅ bases of the SRC	Set Ω_0 of operational states of CTs of the fault-tolerant CS	The first level of degradation (D ₁ = 139)		The second level of degradation (D ₂ = 61)	
23	3	4	5	7				Correlation of bases of the SRC	Ω_1	Correlation of bases of the SRC	Ω_2
1					2	3	4	5	6	7	8
0	0	0	0	0	-	-	+	-	+	-	+
0	0	0	0	1	4	7<23	+	23·3·4·5>139	+	23·3·4·5>61	+
0	0	0	1	0	3	5<23	+	23·3·4·7>139	+	23·3·4·7>61	+
0	0	0	1	1	3, 4	5·7>23	-	23·3·4·>139	+	23·3·4>61	+
0	0	1	0	0	2	4<23	+	23·3·5·7>139	+	23·3·5·7>61	+
0	0	1	0	1	2, 4	4·7>23	-	23·3·5>139	+	23·3·5>61	+
0	0	1	1	0	2, 3	4·5<23	+	23·3·7>139	+	23·3·7>61	+
0	0	1	1	1	2, 3, 4	4·5·7>23	-	23·3<139	-	23·3>61	+
0	1	0	0	0	1	3<23	+	23·4·5·7>139	+	23·4·5·7>61	+
0	1	0	0	1	1, 4	3·7<23	+	23·4·5>139	+	23·4·5>61	+
0	1	0	1	0	1, 3	3·5<23	+	23·4·7>139	+	23·4·7>61	+
0	1	0	1	1	1, 3, 4	3·5·7>23	-	23·4<139	-	23·4>61	+
0	1	1	0	0	1, 2	3·4<23	+	23·5·7>139	+	23·5·7>61	+
0	1	1	0	1	1, 2, 4	3·4·7>23	-	23·5<139	-	23·5>61	+
0	1	1	1	0	1, 2, 3	3·4·5>23	-	23·7>139	+	23·7>61	+
0	1	1	1	1	1, 2, 3, 4	3·4·5·7>23	-	23<139	-	23<61	-
1	0	0	0	0	5	3·4·5·7=420	+	3·4·5·7>139	+	3·4·5·7>61	+
1	0	0	0	1	5, 4	-	-	3·4·5<139	-	3·4·5<61	-
1	0	0	1	0	5, 3	-	-	3·4·7<139	-	3·4·7>61	+
1	0	0	1	1	5, 3, 4	-	-	3·4<139	-	3·4<61	-
1	0	1	0	0	5, 1	-	-	3·5·7<139	-	3·5·7>61	+
1	0	1	0	1	5, 1, 4	-	-	3·5<139	-	4·5·7>61	-
1	0	1	1	0	5, 1, 3	-	-	3·7<139	-	3·7>61	-
1	0	1	1	1	5, 1, 3, 4	-	-	3<139	-	3<61	-
1	1	0	0	0	5, 1	-	-	4·5·7>139	+	4·5·7>61	+
1	1	0	0	1	5, 1, 4	-	-	4·5<139	-	4·5<61	-
1	1	0	1	0	5, 1, 3	-	-	4·7<139	-	4·7>61	-
1	1	0	1	1	5, 1, 3, 4	-	-	4<139	-	4<61	-
1	1	1	0	0	5, 1, 2	-	-	5·7<139	-	5·7>61	-
1	1	1	0	1	5, 1, 2, 4	-	-	5<139	-	5<61	-
1	1	1	1	0	5, 1, 2, 3	-	-	7<139	-	7<61	-
1	1	1	1	1	1, 2, 3, 4, 5	-	-	-	-	-	-
							$\Omega_0=10$			$\Omega_1=14$	$\Omega_2=19$

Variant 1.3. The control CT 2₅ is operational; however, some information CTs have failed.

Variant 1.3.1. Suppose CTs by the bases m₁ and m₂ have failed i.e., tracks 2₁ and 2₂. The binary code representing the states of CTs 2₁-2₅, 01100, is transmitted through buses 16₁÷16₅ to the input of decoder 7. The signal from its output goes through the twelfth output bus via OR elements 8 and 14

to the "OPERATIONAL" output 15 (see Table 2, columns 1-4). Concurrently, the signals the code 01100 activate AND elements 4₁ and 4₂. The signal from bus 17, firstly, goes through OR elements 5₁ and 5₂ to the "STOP" inputs, disabling CTs 2₁ and 2₂. Secondly, it goes through OR element 6 to the "START" input of the control CT 2₅. Consequently, the fault-tolerant CS remains operational; the information is processed by CTs 2₃+2₅.

Variant 1.3.2. Suppose CTs 2₃ and 2₄ failed. The binary code representing the states of CTs 2₁₋₂₅, 00011, is transmitted via buses 16_{1÷165} to the input of the decoder 7. The signal from its output (second group of outputs from decoder 7) goes through the third bus via OR element 9 (second group of outputs, see Table 2, column 4, "-" symbol), activating the first AND element 13₁ of the group (control signal of the first level of degradation). In this case, the fault-tolerant CS operates at the first level of degradation mode.

Variant 1.4. One or several informational CTs 2₁₋₂₄ and control CT 2₅ simultaneously failed. In this case, if there is a binary code in the first (left) position (control CT 2₅ has failed) and an additional presence of a unit (one) in an arbitrary position of the output binary code of output bus signals 16_{1÷165}, all CTs 2_{1÷25} are stopped, i.e. the fault-tolerant CS in the SRC is inoperable. In this case, the fault-tolerant CS will function in the second degradation mode.

Let us consider the second (with degradation) mode of functioning of the fault-tolerant CS. Assume the device operates at the second level ($D_2 = 61$) of degradation. Accordingly (see Table 2, columns 1, 7 and 8), the first group of outputs of decoder 10₂ unifies a set of buses corresponding to the operational states $\Omega_2=19$ of the second level of degradation (Table 2, column 8, sign "+"), and the second group of outputs unifies the set of buses corresponding to inoperable states (see Table 2, column 8, sign "-").

Variant 2.1. CTs 2₁, 2₂ and 2₃ failed. The binary code representing the states of CTs 2₁₋₂₅, 01110, is transmitted through buses 16_{1÷165} to the input of decoder 10₂ (see Table 2, columns 1, 7, and 8). The signal from its output goes through the fourteenth bus (first group of decoder outputs 10₂) via AND elements 11₂, 13₂ and 14 go to the "OPERATIONAL" output 15 of the fault-tolerant CS.

Variant 2.2. CTs 2₁, 2₂, 2₃ and 2₄ have failed. The binary code representing the states of CTs 2₁₋₂₅, 01111, is transmitted through buses 16_{1÷165} to the input of the decoder 10₂ (see Table 2, columns 1, 7, and 8). The signal from its output goes through the fifteenth bus (second group of decoder outputs 10₂) via AND elements 12₂ and 5_{1÷55} go to the second inputs of all CTs 2₁₋₂₅ of the fault-tolerant CS. In this case, the "OPERATIONAL" signal from bus 15 is absent, meaning that the fault-tolerant CS in the SRC is inoperable.

From the given example, it is obvious that the non-positional numbering system in residual classes is an effective tool for increasing the fault tolerance of the CS.

6. Results and Discussion

Based on the results of the research conducted in this article, it can be asserted that the uniqueness of the fault-tolerant functioning of the CS in the SRC is due to the influence of the primary properties of the non-positional number system, which are as follows:

1. The principles of building the structures of the non-positional code created the basis for ensuring the reliable work of the CS in the SRC.

2. In SRC, the application of one type of reservation causes the simultaneous presence of other types of reservation, i.e., it causes other types of redundancy. Thus, the use of information reservation (the introduction of information redundancy due to the introduction of control bases) to increase the reliability of calculations leads to the presence of structural redundancy, which can be additionally used to increase resistance to failure of the CS. During the implementation of the method of passive or active fault tolerance method, the essence of which is to identify (determine) the NR of the CS by using the applied number system. With the joint use of NR and AR, based on known methods of increasing reliability, the maximum value of non-failure of CS due to the total over-dimension can be achieved. It should be noted that in SCR primary structural redundancy is significantly manifested only in the presence of secondary structural redundancy.

3. When secondary structural redundancy is introduced into the CS, the primary structural redundancy is also significantly manifested, caused by the formation of codes in the SRC. In this case, the fault tolerance of the CS in the SRC can be explained as follows. Based on the property of the SRC, each residue of a number in the SRC carries information about the entire original number. This in PNS is equivalent to the fact that, as if, smaller nodes of the CS are reserved. According to the general theory of reliability, it is advisable to reserve small nodes and blocks of a complex system to increase fault tolerance. For SRC, the roles of individual blocks and nodes should be considered as separate computational tracts of the CS. In this case, the probability of fault-free operation of the CS in the SRC, with the reservation of computational paths, is higher than the probability of fault-free operation of the CS in the PNS with a triple majority structure (a triple computing system).

4. A direct analogy of the structure of the CS in the SRC with the structure of the reserved CS in the PNS, this circumstance, using the approaches and mathematical relations known in the theory of reliability for the appropriate methods of reservation in the PNS will allow synthesizing a set of mathematical models for conducting a quantitative assessment and comparative analysis of the fault tolerance of the CS in the SRC.

The results of the analysis of the example of the functioning of the fault-tolerant CS in the SRC given in the article, given by four information bases and only one control base, showed that the use of the SRC provides a greater number of operational states of CS with reduced quality (greater number of degradation levels) of functioning than the total number of operational states of CS in the PNS.

The enhancement of fault tolerance in CS is conditioned by the utilization of the basic qualities of the SRC. The compromise for increasing CS fault tolerance through the application of SRC is as follows:

1. Significant efficiency from using SRC in CS is realized only when processing integers.
2. There is a temporal and technical complexity involved in implementing positional operations (such as numerical comparison, control and diagnostics operations, data control, etc.) in the SRC [21].
3. An increased quantity of hardware for non-redundant CS in the SRC is required when compared to the hardware count for CS in the PNS at the same level of fault tolerance.
4. The performance reserve of CS in the SRC for implementing arithmetic operations can be harnessed to enhance fault tolerance, although this could result in some reduction in the speed of arithmetic operations.

These compromises could be used in designing fault-tolerant and high-performance CS in the SRC.

Conclusions

The proposed method for increasing the fault tolerance of the CS is based on the use of existing PR and the presence of the used NS. The concept assumes that at the design stage of the CS, there is the possibility of using the NR (due to the use of NS) and the AR (due to the use of reservation methods). The basis of these methods constitutes the methods of active and passive fault tolerance, which are based on the joint use of NR and AR. This circumstance makes it possible to set and solve the tasks of achieving the required level of reliability at the design stage of the CS for any NS in a new way.

The non-positional number system in residual classes is an effective means of increasing the fault tolerance of CS. This is due primarily to the initial structure of the CS in the SRC (without introducing additional redundancy) has a prior predisposition to the possibility of fault tolerance functioning of the CS. This is due to the effect of the basic qualities of the SRC on the structure of the CS, which is similar to the structure of multi-processor CS in the PNS.

Thus, the proposed option for choosing the form of data encoding (choice of NS) according to criterion (5) allows to create fault-tolerant computing structures (in

particular, CS in the SRC), which ensures fault tolerance functioning of CS in the SRC.

This simultaneous organization of various types of reservations in the SRC, due to the introduction of structural redundancy, is characteristic of the structural and functional organization of human brain activity and can ensure extremely high fault tolerance of computing structures, as well as high processing speed of huge arrays of information. In this aspect, the activity of the human brain is close to the holographic principles of information processing, which, in turn, is consistent with the methods and algorithms of processing in the SRC.

Some theoretical results obtained in this article may contribute to the solution of the problem of developing models and methods for increasing the fault tolerance of CS and CCS operating in the SRC, without reducing the speed of implementation of integer arithmetic operations in computer machine arithmetic of the SRC.

Future Research Development: Further research may be related to the study of the effect of fault tolerance on the survivability of the functioning of a real-time CS. In addition, fault tolerance can be characterized as the ability of a CS to maintain its reliability (availability and sustainability) in the event of failures of its individual elements. In this regard, for a comparative analysis of the characteristics of the CS, further studies should consider in detail the indicators for the quantitative assessment of fault tolerance, reliability, availability, and sustainability.

Contributions of authors: analytical review and analysis of information sources – **Alina Yanko**; statement of the problem and formulation of the research purpose – **Viktor Krasnobayev**; conceptualization, methodology – **Viktor Krasnobayev**; calculations and description of the result – **Anatolii Martynenko**; analysis of results and formation of research conclusions – **Viktor Krasnobayev**; writing – original draft preparation, writing – review and editing – **Alina Yanko**.

All authors have read and agreed to the published version of this manuscript.

References

1. Medero, A., & Puig, V. LPV Control and Virtual-Sensor-Based Fault Tolerant Strategies for a Three-Axis Gimbal System. *Sensors*, 2022, vol. 22, iss. 17, article no. 6664, pp. 1-25. DOI: 10.3390/s22176664.
2. Omondi, A. R. *Cryptography Arithmetic: Algorithms and Hardware Architectures*. Springer, Cham, 2020. 336 p. DOI: 10.1007/978-3-030-34142-8.
3. Krasnobayev, V., Kuznetsov, A., Yanko, A. & Kuznetsova, T. The Procedure for Implementing the

Operation of Multiplying Two Matrices Using the Residual Number System. *2020 IEEE International Conference on Problems of Infocommunications. Science and Technology (PIC S&T)*, Kharkiv, Ukraine, 2020, pp. 353-357. DOI: 10.1109/PICST51311.2020.9468076.

4. Hiasat, A. General Frameworks for Designing Arithmetic Components for Residue Number Systems. *Intelligent Methods in Computing, Communications and Control (Advances in Intelligent Systems and Computing)*, 2021, vol. 1243, pp. 82-92. DOI: 10.1007/978-3-030-53651-0_7.

5. Koshman, S. O. *Metody ta zasoby operatyvnoho kontrolyu ta diahnostryky danykh komponentiv komp'yuternoyi systemy u zalyshkovykh klasakh. Diss. d. t. n.* [Methods and tools for operative data verification and diagnosis of computer system components in residue classes. Doctor of Technical Science diss.]. Kharkiv, 2018. 340 p. (In Ukrainian).

6. Pradhan, D. K. *Fault-Tolerant Computer System Design*. 1st ed. Prentice Hall, Upper Saddle River, N.J, 1996. 550 p.

7. Castaldi, P., Mimmo, N., & Simani, S. Fault diagnosis and fault-tolerant control techniques for aircraft systems. *Fault Diagnosis and Fault-tolerant Control of Robotic and Autonomous Systems*. London, 2020, pp. 197-212. DOI: 10.1049/PBCE126E_ch9.

8. Hajiyeve, Ch., & Soken, H. E. Active Fault Tolerant Attitude Estimation. *Fault Tolerant Attitude Estimation for Small Satellites*. 1st ed. CRC Press, 2020, pp. 175-198. DOI: 10.1201/9781351248839.

9. Selianinau, M. An efficient implementation of the CRT algorithm based on an interval-index characteristic and minimum-redundancy residue code. *International Journal of Computational Methods*, 2020, vol. 17, no. 10. DOI: 10.1142/S0219876220500048.

10. Selianinau, M. An efficient implementation of the Chinese Remainder Theorem in minimally redundant Residue Number System. *Computer Science*, 2020, vol. 21, no. 2, pp. 237-252. DOI: 10.7494/csci.2020.21.2.3616.

11. Phalakarn, K., & Surarerks, A. Alternative Redundant Residue Number System Construction with Redundant Residue Representations. *2018 3rd International Conference on Computer and Communication Systems (ICCCS)*, Nagoya, Japan, 2018, pp. 457-461, DOI: 10.1109/CCOMS.2018.8463305.

12. Molahosseini, A., Sousa, L., & Chang, C. *Embedded Systems Design with Special Arithmetic and Number Systems*. Springer, Cham, Switzerland, 2017. DOI: 10.1007/978-3-319-49742-6.

13. Babeshko, E., Kharchenko, V., Leontiev, K., & Ruchkov E. Practical aspects of operating and analytical reliability assessment of FPGA-based I&C systems. *Radioelectronic and Computer Systems*, 2020, no. 3, pp. 75-83. DOI: 10.32620/reks.2020.3.08.

14. Kharchenko, V., Fesenko, H., & Illiashenko, O. Basic model of non-functional characteristics for assessment of artificial intelligence quality. *Radioelectronic and Computer Systems*, 2022, no. 3, pp. 131-144. DOI: 10.32620/reks.2022.2.11.

15. Makarichev, V., & Kharchenko, V. Application of dynamic programming approach to computation of atomic functions. *Radioelectronic and Computer Systems*, 2021, no. 4, pp. 48-62. DOI: 10.32620/reks.2021.4.03.

16. Osamy, W., Khedr, A. M., Salim, A., El-Sawy, A. A., Alreshoodi, M., & Alsukayti, I. Recent Advances and Future Prospects of Using AI Solutions for Security, Fault Tolerance, and QoS Challenges in WSNs. *Electronics*, 2022, vol. 11, no. 24, article no. 4122. DOI: 10.3390/electronics11244122.

17. Wu, Y., Jiang, B., & Wang, Y. Incipient winding fault detection and diagnosis for squirrel-cage induction motors equipped on CRH trains. *ISA Transactions*, 2020, vol. 99, pp. 488-495. DOI: 10.1016/j.isatra.2019.09.020.

18. Barbirotta, M., Cheikh, A., Mastrandrea, A., Menichelli, F., Ottavi, M., & Olivieri, M. Evaluation of Dynamic Triple Modular Redundancy in an Interleaved-Multi-Threading RISC-V Core. *Journal of Low Power Electronics and Applications*, 2023, vol. 13, no. 1. DOI: 10.3390/jlpea13010002.

19. Al-Zuriqat, T., ChillónGeck, C., Dragos, K., & Smarsly, K. Adaptive Fault Diagnosis for Simultaneous Sensor Faults in Structural Health Monitoring Systems. *Infrastructures*, 2023, vol. 8, no. 3. DOI: 10.3390/infrastructures8030039.

20. Fu, H.-W., Chen, T.-Y., Shen, M.-W., & Huang, T.-C. AN-Coded Redundant Residue Number System for Reliable Neural Networks. *2021 IEEE International Conference on Consumer Electronics-Taiwan (ICCE-TW)*, Taiwan, 2021, pp. 1-2. DOI: 10.1109/ICCE-TW52618.2021.9603049.

21. Krasnobayev, V. A., Yanko, A. S., & Kovalchuk, D. M. Control, Diagnostics and Error Correction in the Modular Number System. *Proceedings of The Sixth International Workshop on Computer Modeling and Intelligent Systems (CMIS 2023)*, Zaporizhzhia, Ukraine, 2023, pp. 199-213. DOI: 10.32782/cmisi/3392-17.

22. Taghizadeghankalantari, M., & TaghipourEivazi, S. Design of efficient reverse converters for Residue Number System. *Journal of Circuits, Systems and Computers*, 2021, vol. 30, no. 8. DOI: 10.1142/S0218126621501413.

23. Barannik, V., Krasnorutsky, A., Kolesnyk, V., Barannik, V., Pchelnykov, S., & Zeleny, P. Method of compression and ensuring the fidelity of video images in infocommunication networks. *Radioelectronic and*

Computer Systems, 2022, no. 4, pp. 129-142. DOI: 10.32620/reks.2022.4.10.

24. Krasnobayev, V. A., Zamula, O. A., Rassomakhin, S. H., Styervoyedov, M. H., & Kurchanov, V. M.

Vidmovostiyy obchyslyval'nyy prystriy, shcho funktsionuye u systemi zalyshkovykh klasiv [A fault-tolerant computing device operating in a system of residual classes]. Patent UA, no. 122286, 2020.

Received 28.07.2023, Accepted 20.09.2023

ВПЛИВ СИСТЕМИ ЧИСЛЕННЯ В ЗАЛИШКОВИХ КЛАСАХ НА ВІДМОВСТІЙКІСТЬ КОМП'ЮТЕРНОЇ СИСТЕМИ

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Предметом статті є методи та засоби підвищення відмовостійкості комп'ютерної системи (КС) та компонент на основі використання непозиційної системи числення в залишкових класах. Розглянуто нову концепцію підвищення відмовостійкості КС за рахунок використання наявної надмірності, що утворюється від застосовуваної системи числення. Показано, що використання системи залишкових класів (СЗК), як системи числення, дозволяє забезпечувати відмовостійке функціонування КС реального часу. У цій статті розглядається відмовостійка КС, що функціонує в СЗК. Мета дослідження – забезпечення відмовостійкого функціонування КС реального часу на основі використання непозиційної системи в залишкових класах. Об'єкт досліджень – процес обробки даних, представлених у непозиційній системі в залишкових класах. У статті наведено приклад функціонування відмовостійкої КС у СЗК, заданої набором конкретних основ. Відмовостійкість КС у СЗК забезпечується за рахунок використання основних властивостей СЗК, способом активної відмовостійкості, шляхом використання процедури поступової деградації. Рівень відмовостійкості КС у СЗК у наведеному в статті прикладі досягається за рахунок зниження точності обчислень. У статті розглядається два рівня деградації. Наведено варіанти алгоритмів функціонування відмовостійких КС у СЗК у режимах заміни та поступової деградації. В основу проведених досліджень були покладені методи: системного аналізу, теорія чисел, теорія обчислювальних процесів та систем, а також теорія кодування у СЗК. Результати аналізу наведеного у статті прикладу функціонування відмовостійкої КС у СЗК, заданої чотирма інформаційними основами і лише однією контрольною основою, показали, що використання СЗК забезпечує більшу кількість працездатних станів КС зі зниженою якістю функціонування, ніж загальна кількість працездатних станів КС у позиційній системі числення. Висновки. У статті запропоновано нову концепцію підвищення відмовостійкості КС, що заснована на використанні наявної первинної надмірності, що міститься в КС, і обумовлену використанням непозиційної системи в залишкових класах.

Ключові слова: обчислювальний тракт; відмовостійкість; відмовостійка комп'ютерна система; система числення; первинна надмірність; методи резервування; система залишкових класів.

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